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China

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SCIENCE & TECHNOLOGY

CHINA

CONTENTS

S&T Cooperation With Mongolia Begins

40101027 Ulaanbaatar International Service in English 1405 GMT 8 Jul 89

[Text] China expresses the hope on further development of scientific and technological cooperation with the Mongolian People's Republic, said member of the State Council of China, Chairman of the State Committee for Science and Technology Song Jian, meeting a Mongolian delegation which has come to Beijing for bilateral talk on further cooperation between China and Mongolia for the period between 1989 and 1990.

This was the first visit of a Mongolian delegation in this sphere after the restoration of scientific and technological ties between the two countries.

Metal-Organic Chemistry Lab Built in Shanghai

40101029 Beijing XINHUA in English 0056 GMT 24 Aug 89

[Text] Beijing, August 24 (XINHUA)--A laboratory for metal-organic chemistry research has recently been built in Shanghai by the Chinese Academy of Sciences and is scheduled to open to Chinese and foreign scientific researchers in December.

The main orientation of the lab is to research on composition, structure, and reactivity in metal organic-chemistry; research on guiding organic composition reaction, as well as finding applications for metal organic chemistry in the materials science and other high technology fields.

The lab is located in the compound of the Shanghai Institute of Organic Chemistry.

Hubei Produces Nontoxic Mosquito Killer

40101031a Beijing XINHUA in English 1503 GMT 22 Aug 89

[Text] Wuhan, August 22 (XINHUA)--A new and highly effective mosquitocide was recently developed here.

The bio-product, which is called highly-effective wiggler-killing biocide, is not harmful to humans or livestock and it does not pollute the environment.

The insecticide was developed jointly by the Huazhong (Central China) Agriculture University and the office of the Hongan County Committee in charge of the Patriotic Health Campaign in Hubei Province.

The mosquitocide is produced by fermenting the ingredients which include wheat bran, rice bran, husk of rice, and peanut cake. These ingredients are readily available year round.

'Significant Progress' in Developing Anti-Cancer Drug Reported

40101031b Beijing XINHUA in English 0727 GMT 10 Sep 89

[Excerpts] Beijing, September 10 (XINHUA)--Chinese biologists have made significant progress in developing a marketable generation of recombinant interferon, a protein which is believed to be effective to the treatment of chronic hepatitis B, some cancers, and many viruses.

Addressing a national meeting on biotechnology, Professor Hou Yunde, China's top molecular virologist and head of the Research Institute of Virology under the Chinese Academy of Preventive Medical Science, disclosed that a research group led by him has finished clinical trial of human alpha-interferon for treatment of viral hepatitis and chronic cervicitis.

The newly-developed interferon will be marketed before the end of this year, according to Professor Hou.

As China's first generation of biotechnology drugs, the newly-developed interferon, many scientists believed, marked a breakthrough in China's high-technology development, and it will bring huge economic benefits to the country. [passage omitted]

At present, China has two labs producing the drug, one in Shanghai and the other in northeast China's Changchun.

Storage for Nuclear Waste Materials Under Construction

40101026 Beijing XINHUA in English 0108 GMT 5 Aug 89

[Text] Beijing, August 5 (XINHUA)--China is building storage facilities for radioactive waste in all the mainland provinces and regions except Hainan and the Tibet Autonomous Region, "CHINA DAILY" reports today.

These facilities, to be completed by the end of 1990, will help control the discharge of radioactive waste produced by 1,000 industrial branches and research establishments across the country, said Luo Guozhen, an official from the State Environmental Protection Bureau.

More than 1,200 people in China had been injured by radioactivity between 1980 and 1985. Yet no more than 20 people died in those calamities, said Luo.

Radioactive waste storage sites have already been built in 12 of the country's municipalities, provinces and autonomous regions.

And radioactive storage will also be built in eight other provinces.

Radioactive leaks in recent years might have been avoided if strict measures on handling radioactive substances had been in effect.

These accidents were caused by managers ignoring the regulations governing radioactive materials as well as by people's ignorance on the subject.

The "CHINA ENVIRONMENTAL NEWS" recently reported a radioactive leak at the Nantong Electronic Textile Equipment Plant in Nantong City, Jiangsu Province.

On December 26, a lead container for Cobalt 60, a radioactive material, was reported missing.

A carpenter at the plant had stolen the container and sold it after emptying its radioactive contents.

So far, no death or injuries have been reported by the plant.

Sichuan Pollution Problem Worsens, Alarms Raised

40101030 Beijing XINHUA in English 0818 GMT 16 Aug 89

[Excerpts] Beijing, August 16 (XINHUA)--Environmental pollution is worsening and threatening the lives of the 100 million people in Sichuan Province.

It is reported that nearly 10,000 people in Hefeng Township, Shifang County were sick, with some showing symptoms such as swelling, skin ulcers and inflammation. Many animals have died after drinking polluted water. Groundwater has been contaminated by a pesticide factory in the township. [passage omitted]

More common is air and water pollution which has destroyed trees and plants, made rivers black and smelly, decimated fish and other organisms, and made life extinct in some rivers.

Local environmental protection departments report that the concentration of pollutants in the Sichuan basin is three times the national average and seven times the global level. The sulphur dioxide emitted by local sulphur plants is equal to spraying 200,000 tons of concentrated sulphuric acid in the province each year. The more than 500 million tons of industrial sludge and garbage in Sichuan occupies 2,700 hectares of land.

The forested area has dropped from 20 percent of the province to 13 percent over the past three decades, while the felling pace has accelerated. At the current felling rate, the province will be completely denuded in 20 years.

Mudflow, which occurred in only 14 counties in the 1930's, affects 135 counties now, resulting in over 10,000 disasters and economic losses of over 100 million yuan.

The paper noted that some departments and local governments, eager for quick benefits, neglect consequences and develop their economies at the expense of the environment.

The provincial government has recently urged local governments at all levels to work out plans for environmental protection and pollution control and required local officials to accomplish them.

CCD/Microcomputer-Based Fringe Processing System Announced

40080202 Beijing YIQI YIBIAO XUEBAO [CHINESE JOURNAL OF SCIENTIFIC INSTRUMENT] in Chinese Vol 10 No 2, May 89 pp 151-156

[Article by Chen Xi [7115 1585], Hu Xiaotang [5170 1420 0781], Feng Keyou [7458 0344 3731], and Ye Shenghua [0673 5116 5478], Tianjin University, Department of Precision Instrument Engineering: "A CCD-Microcomputer-Based Constant-Angle Laser Interferometer Fringe Processing System"; manuscript received Feb 88]

[Text] A constant-angle interference fringe processing system for use in laser-interferometer arbitrary angle-measurement systems is described. In this system we use multi-cycle spaced sampling to enable the CCD [charge-coupled device] signal data rate to coincide with the data collection rate of the Apple II microcomputer; we have used the RDY interface to enable the data collection system to have an external toggle function, as well as to approximate the ultimate data collection rate of the Apple II in non-DMA [direct memory access] mode; using two interference-fringe digital signal processing methods--the optimized method and the DFT [discrete Fourier transform] method--this system is suited for both widely spaced and tightly spaced interference fringe measurement. This system has higher measurement precision and stronger anti-interference capabilities.

I. Introduction

What is meant by "constant angle" is the optical component formed by the arrangement of two surface reflectors arranged at a particular included angle β. The constant angle that is one odd-numbered part of the angle value π is called the standard constant angle, denoted as β_S. According to the constant-angle interference measurement theory [1], the standard-angle interference fringes are the two sets of isopach interference fringes that are parallel to intersecting edges of the constant angle, and they are at fringe spacing. The deviation $\Delta\beta$ between the constant angle value β and the standard constant angle value β_S can be calculated from the widths e_a and e_b of the two sets of fringe. e_a and e_b have the following relationship to $\Delta\beta$:

$$\Delta\beta = \frac{\lambda}{2(2m-1)}(1/e_a - 1/e_b) \quad (1)$$

where λ is the laser wavelength and m is the positive integer determined by the size of β.

The traditional interference-fringe spacing [i.e., interval] measurement method is where a sighting is taken on two corresponding characteristic points in the fringe at two separate instances, and the numbers read. This measurement method allows the introduction of errors from human subjective interpretation. Additionally, the effects of atmospheric agitation, temperature-gradient changes, and oscillation will cause drift and deformation, and will also generate measurement errors. What is described in this paper is an interference-fringe processing system that is composed of a CCD and a microcomputer, and that can very quickly capture light intensity distribution data from the entire interference field. It also uses optimized processing methods and DFT processing methods to eliminate and suppress various effects of signal errors, which strengthens the system anti-interference capacity and overcomes the deficiencies of the traditional method, thereby improving measurement precision.

II. System Hardware Structure

1. Hardware Structure

A key block diagram of the measurement system is shown in Figure 1. There are four parts to the system hardware: 1) the CCD and its driver circuitry and the video amplification circuitry; 2) interval-sampling synchronization circuitry; 3) data-acquisition interface circuitry; and 4) the microcomputer system.

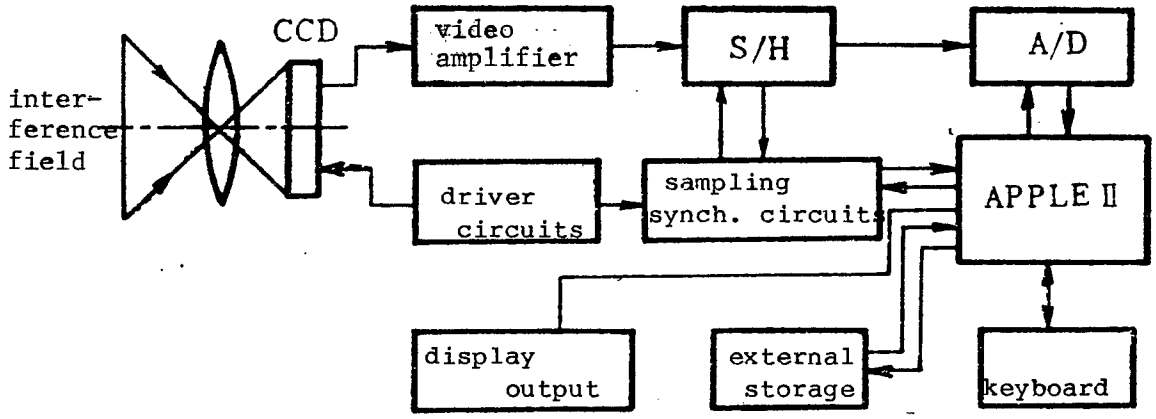

Figure 1. Principles of the Measurement System

The CCD uses a 1,728-bit linear-array device, with a pixel spacing of 12 microns. The driver circuitry generates a CCD working pulse and output synchronization pulses, with an operating frequency of 100 kHz; the output synchronization pulses provide the spacing-sampling synchronization circuitry. The video amplification circuitry enlarges to a certain amplitude the video voltage signals output by the CCD, which facilitates A/D

conversion. Among its features is that D.C. floating is adjustable for differential input, broad-band, and output-voltage signals. The Apple II is used as the microcomputer. It has an operating clock frequency of 1 MHz, with real-time screen display of the interference fringe pattern; measured results are automatically printed out.

The spacing-sampling synchronization circuitry and the data-acquisition interface circuitry are the core of the system hardware.

2. Spacing-Sampling Synchronization Circuitry

The video signal data rate is determined by the CCD driving pulse and equals 100 kHz. Because of interference by thermal noise on the injected signal, lowering the driving-pulse frequency will cause a clear drop in output signal quality. On the other hand, the clock speed of the 6502 CPU is 1 MHz, and in general one read-write instruction requires 4-6 microseconds. If we use an A/D converter with a conversion time of 2.5 microseconds and 12-bit resolution, through close integration of the hardware and software, data-acquisition time can be around 50 microseconds. Obviously, the CCD video signal data rate is greater than the data-acquisition rate of the computer. To resolve this contradiction without losing the CCD space resolution, we have designed spacing-sampling synchronization circuitry to implement multi-cycle scanning spacing sampling.

The core of the spacing-sampling synchronization circuitry consists of pre-settable adders and subtracters, which constitute the pulse erasure circuit and serve the function of continuously erasing the 0--N-1 pulses at N scanning cycles. Within the stop-scanning time, as each cycle begins, the adder adds 1, continuing until it reaches the state value set by the subtracter. Then, the subtracter begins erasing the sampling pulse when the scanning begins. When erasure concludes, the iso-border N frequency divider begins a sampling pulse frequency division for each scan cycle. The iso-border N frequency divider is an N frequency divider in which, when the first input pulse arrives, the output terminal can generate a jump [in frequency]. In short, the pulse-erasure circuit determines the frequency division starting point of the sampling pulse by the iso-border N frequency divider at each scan cycle, and the iso-border N frequency divider serves to widen the sampling pulse spacing N-1 times. The output of this circuit acts as the spacing-sampling pulse ϕ_{SH} for the sampling-retention terminal in the data-acquisition interface, the frequency division integer N being arbitrarily selected in the range 0-15.

3. Data-Acquisition Interface Circuitry

Spacing-sampling pulses are equidistant within the same scan cycle, but the last pulse of the previous cycle will be quite distant from the first pulse in the next cycle. For this reason, using this signal as the sampling-retention signal requires that the computer data-acquisition cycle be less than a normal spacing-sampling pulse interval, and also that it be able to adapt to changes in the pulse interval. To meet these requirements, this paper proposes the RDY interface method. This method does not require repetitive polling, both the hardware and software are quite simple, and

completing one wait period saves 6-10 microseconds over the polling method, which then improves the data-acquisition rate. By "RDY interface method" we mean using the hardware wait function of the 6502 CPU's RDY line, an interfacing method that transfers peripheral status information.

The data-acquisition interface using the RDY interfacing method, with external trigger function, is shown in Figure 2. The interface circuitry includes two indicator ports that use the RDY interface method: the holding indicator port and the conversion indicator port. The indicator status lines are all interconnected via a tri-state buffer and the RDY terminal of the 6502 CPU. The enable terminal of the tri-state buffer is connected to the corresponding output terminal of the address decoder. Whenever a "read indicator port" instruction is executed, the corresponding indicator port becomes ready.

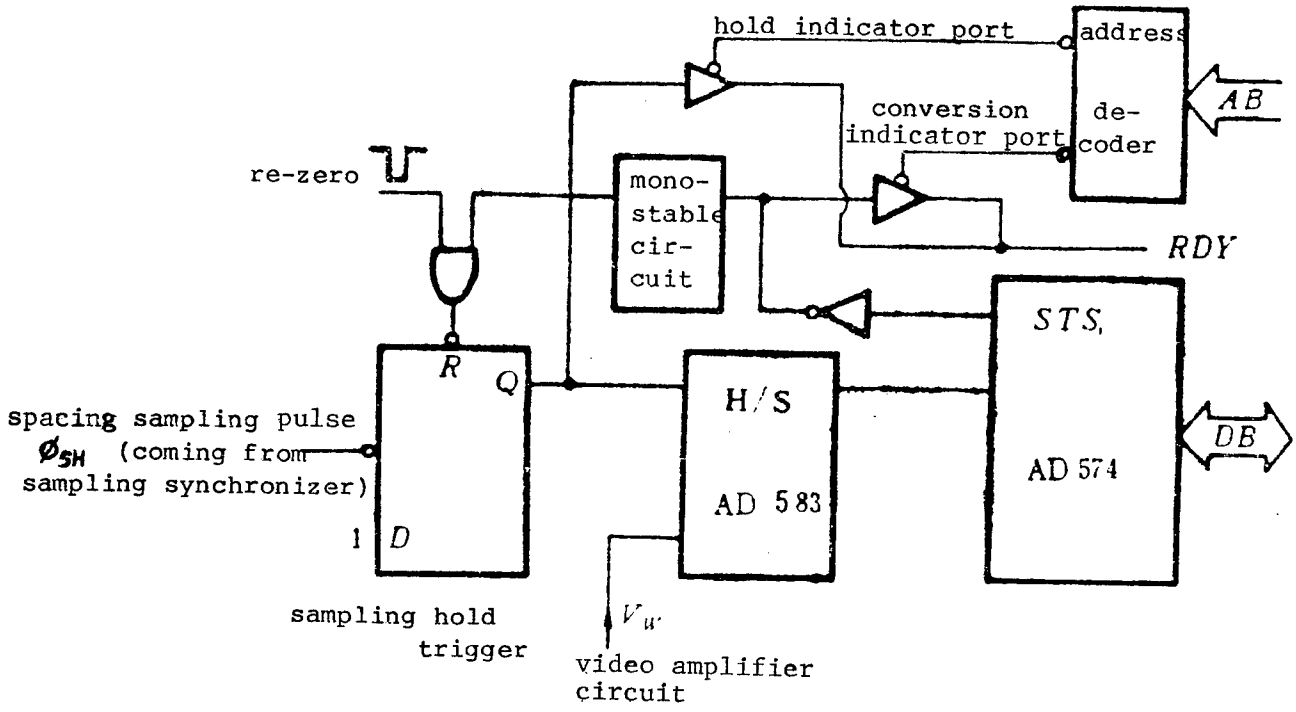

Figure 2. Data-Acquisition Interface

The A/D converter is an AD574, with conversion time of 25 microseconds. An AD583 is used for the sampling retention device. When the sampling pulse arrives, the sampling-retention trigger flips, causing the AD583 to go into a holding state, and the software activates the AD574. After conversion, the STS jumps back to a low state, a monostable trigger re-zeroes the sampling-retention trigger, and the AD583 returns to its sampling state.

A data-acquisition assembly language program was written in accordance with the data-acquisition interface hardware shown in Figure 2, a flowchart for which is shown in Figure 3. In designing the program, a portion of RAM and modified address pointers, as well as identification and end operations are

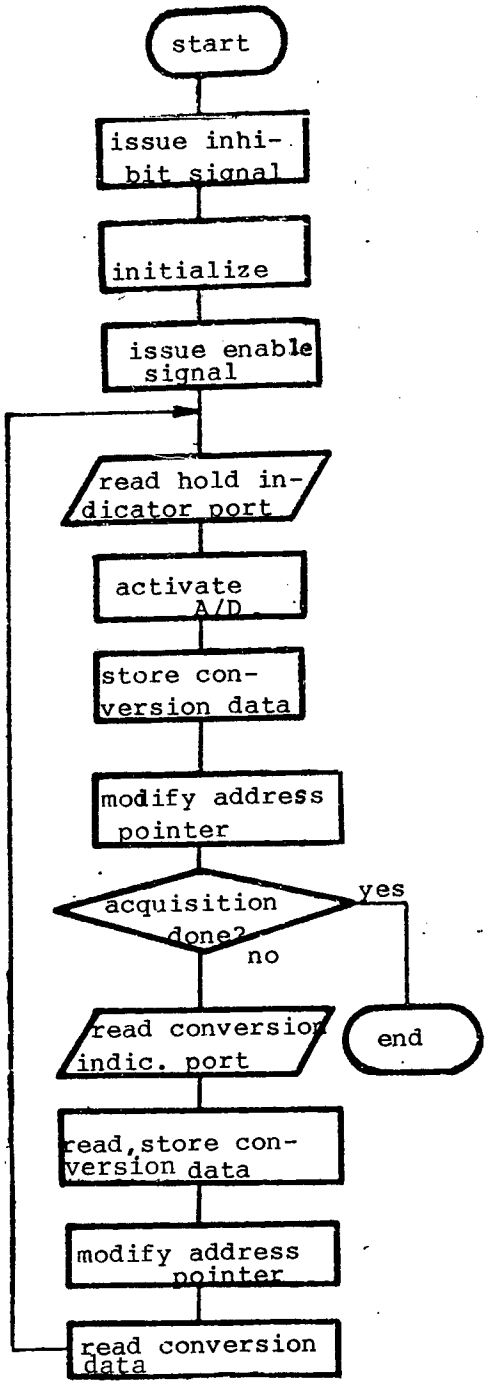

Figure 3. Flowchart for Data Acquisition Routine

set within the 25 microseconds it takes the AD574 to convert, which improves the data-acquisition rate. When the frequency division value N for the spacing-sampling synchronizing circuitry is 5, the data-acquisition rate in real-time measurement is 20 kHz. Under the same hardware conditions, this system approaches the limits of the data-acquisition rate of the Apple II microcomputer using a non-DMA mode.

III. The Processing of Interference-Fringe Data

1. The Pre-Processing of Interference-Fringe Digital Signals

The pre-processing of digital signals primarily includes: the sequential ordering of data, the correction of irregularities in CCD pixel light sensitivity, and digital smoothing filtering. Among these, the former two pre-processing steps are accomplished by the assembly language program. The digital smoothing filter smooths 5.3 times, which is done in a high-level language.

For the processing of interference-fringe digital signals after pre-processing, both optimized processing methods and DFT processing methods can be used, the former suitable for processing widely spaced interference-fringe data, and the latter for processing tightly spaced interference-fringe data.

2. The Optimized Processing Method

Constant-angle laser interference fringe is planar isopach interference fringe, and considering the Gaussian distribution properties of the laser beam, the theoretical distribution rule [2] for the light intensity of interference fringe is:

$$y = \exp(-x^2/C_1^2)[C_2 + C_3\cos(C_4x + C_5)] \tag{2}$$

where C_i (i = 1,2,...,5) is a constant, and C_4 is the space angle frequency of the interference fringe.

The best solution when solving for the objective function of the data y_i^*

$$\min S = \sum_i [y(x_i;\ \vec{X}) - y_i^*]^2 \tag{3}$$

is

$$\vec{\hat{X}} = (\hat{C}_1,\ \hat{C}_2,\ \hat{C}_3,\ \hat{C}_4,\ \hat{C}_5)$$

where $\vec{X} = (C_1,C_2,C_3,C_4,C_5)$, and the estimated value of $y(x_i; \vec{X})$ is obtained from x in the substitution equation for x_i (2). The interference fringe at spacing of T is

$$T = 2\pi/\hat{C}_4 \tag{4}$$

Normally, it is difficult to solve for the analytical solution of (3). By using the optimized method that is the simplex acceleration method [3], one can quickly solve for the numerical solution.

3. The DFT Processing Method

The convergence success rate of the optimized method is related to the size of the measured interference-fringe spacing, and it is suitable for use in interference-fringe processing at intervals greater than 0.5 mm. Fortunately, the DFT processing method supplements the insufficiencies of the optimized method. It is for use in narrowly spaced interference fringes and has high measurement precision and stronger anti-interference capacity.

In the discrete Fourier frequency spectrum of interference-fringe digital signals, the space frequency corresponding to the maximum value of the spectral amplitude value outside the zero-frequency is treated as the estimated value of the measured interference-fringe spacing frequency. If we use N number of sampling points, and the sampling spacing is Δt, then the interference fringe spacing is

$$T_m = 1/S_m = N \cdot \Delta t / m \tag{5}$$

where m is the spectral gradient of the maximum point placement in the amplitude value in the interference-fringe digital signal discrete Fourier frequency spectrum, and where m does not equal zero. At this time, the theoretical resolution is

$$D_m = N \cdot \Delta t / [2m(m-1)] \tag{6}$$

Further analysis of the theoretical resolution [2] shows that the theoretical resolution when the DFT processing method measures interference-fringe spacing is only related to fringe spacing and the sampling length. When the sampling length is fixed, the denser the fringe, the higher the theoretical resolution; for two identically measured fringes, increasing the sampling length can improve the theoretical resolution.

To improve the theoretical resolution, by the spectral gradient m and the amplitude value information of the surrounding gradients, one can determine the estimated value $\hat{m}_e$ for the interference-fringe spectral gradient by the parabolic value insertion method, solving for the interference fringe spacing with m of the $\hat{m}_e$ substitution expression (5).

IV. System Software

The system software is composed of several modules, which primarily include such subroutines as those for data acquisition, digital signal pre-processing, screen plotting, determination of initial values, solving for spacing with the optimized processing method, solving for spacing with the DFT processing method, and standard constant-angle errors. Among these subroutines, the optimized subroutine uses the simplex acceleration optimization method, and

the DFT calculations use FFT [fast Fourier transform] algorithms. The system software runs on a DOS 3.3 operating system.

V. Conclusions

By use of the multiple-cycle spacing sampling method we can resolve the conflict whereby the CCD signal data rate is higher than the data-acquisition rate of the Apple II microcomputer. Use of the RDY interface mode proposed herein can improve the data-acquisition rate for data-acquisition systems, which allow them to approach the data-acquisition rate limits for the Apple II in non-DMA mode.

Using the optimized and DFT processing methods for interference-fringe digital signal information we can make full use of all the measured data to effectively eliminate the effects of random errors on measurement results, and this also has a suppressing effect on gross errors and isolates errors from harmonic disturbance.

As far as indicating measurement results for constant-angle interference fringe in a laser-interference arbitrary-angle measurement system is concerned, for interference fringe spaced greater than 0.5 mm, the convergence success rate for this measurement system using the optimized method is greater than 95 percent, and measurement precision is better than 4 microns; for interference fringe spaced at less than 0.5 mm, measurement precision is better than 1 micron using the DFT processing method.

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[2] Chen Xi, "Research on Laser Interference Fringe High-Precision Measurement Systems," Ph.D. diss., Tianjin University, 1987, pp 47-77.

[3] T. E. Xiaopu [Sharpe?], "Guide to Computer Methods and Applications," Coal Industry Publishing House, 1985.

Quasi-Planar InGaAsP/InP Heterojunction Bipolar Transistor-Based Optoelectronic Integrated Circuit

40080191a Beijing BANDAOTI XUEBAO [CHINESE JOURNAL OF SEMICONDUCTORS] in Chinese Vol 10 No 3, Mar 89, pp 173-178

[Article by Li Weidan [2621 4850 2481], Fu Xiaomei [1381 1420 1188] and Pan Huizhen [3382 1979 3791] of Shanghai Institute of Metallurgy of the Chinese Academy of Sciences, manuscript received 24 Nov 87: "Quasi-Planar InGaAsP/InP Heterojunction Bipolar Transistor and Integrated Optoelectronic Device"]

[Text] Abstract

The relationship between the structural parameters and performance characteristics of the InGaAsP/InP heterojunction bipolar transistor (HBT) has been studied by computer aided analysis. On this basis, a quasi-planar double collector HBT and its fabrication techniques are presented. The characteristics of this device have been tested and the effect of material quality is discussed. An optoelectronic integrated circuit (OEIC) using this HBT is also introduced in this paper.

Key words: InGaAsP/InP heterojunction bipolar transistor, optoelectronic integrated circuit

A heterojunction bipolar transistor (HBT) has advantages such as high speed, high gain and high current capacity [1,2]. It also has good longitudinal symmetry structurally. Therefore, it is widely used in high-speed integrated circuits (IC) and optoelectronic integrated circuits (OEIC). Due to the high electron mobility of InGaAsP, together with the fact that its optoelectronic characteristics are suitable for fabricating an emitter for long-wavelength optical communications, the development of an InGaAsP/InP HBT has a great deal of potential. Since the advent of the HBT in the 1970's [3,4], many schemes have been presented, including their structures and fabrication techniques [1,2,5,6]; only a few, however, are suitable for InGaAsP/InP IC's and OEIC's. Hence, the relationship between the structural parameters of the InGaAsP/InP HBT and its characteristics and the effects of the planar structure, its fabrication techniques and materials on its performance are urgent matters to be investigated.

The authors employed a computer aided analysis technique to study the relationship between the structural parameters of this HBT and its gain and switching speed in an attempt to develop an InGaAsP/InP OEIC. The effect of major HBT performance parameters on the OEIC frequency response was determined. On this basis, we present a quasi-planar InP-based integrated HBT structure and its fabrication techniques. Such a device was fabricated and studied. Furthermore, the effect of material quality on the performance of the device is discussed.

I. Structural Design of the InGaAsP/InP HBT

Both the longitudinal and transverse structure of an HBT can affect each individual performance characteristic. Here, the two most important parameters, i.e. the current gain Hfe and the transient characteristics, are analyzed.

From the energy-band structure of heterojunction materials, we know that if we choose InP as the wide-band emitter and InGaAsP with E_g = 0.95 eV (300 K) as the base, the emitting efficiency γ of the heterojunction is approximately 100 percent [1]. In this case, Hfe is determined by the HBT base transport efficiency. Figure 1 shows the hyperbolic curves representing the dependence of base transport efficiency upon base width, W_b, at different base minority carrier diffusion lengths, Lnb[7,8]. In addition to the intrinsic properties of the material itself, Lnb is principally determined by dopant concentration, type and lattice integrity. The four conditions shown in Figure 1 are typical values found with p-type liquid phase epitaxially (LPE) grown InGaAsP (λ_g= 1.3 μm, p = 10^{16} - 10^{18} cm^{-3}) with less than 10^{-3} lattice mismatch[9]. From the figure, in the region where W_b is less than 0.3 μm, Hfe is very sensitive to W_b and Lnb when Lnb is around 1.2 μm. If W_b increases from 0.2 μm to 0.3 μm, Hfe decreases by approximately 55 percent. Therefore, it is necessary to choose the proper base structure parameters and techniques based on the design requirement for Hfe.

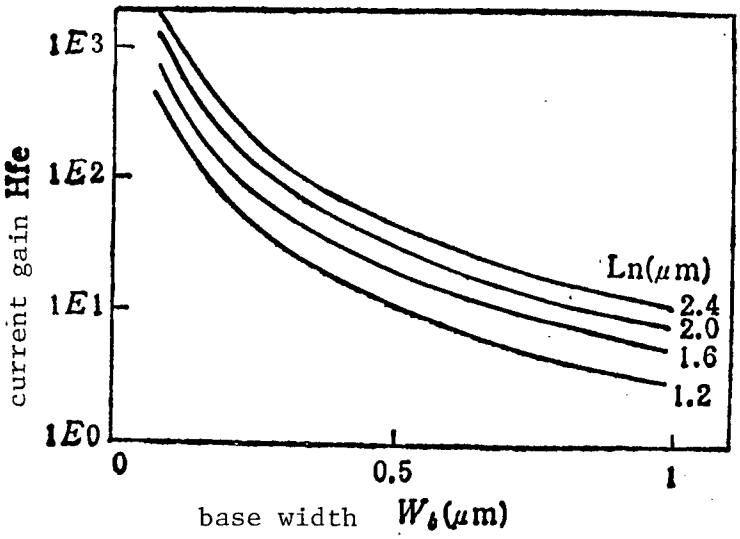

Figure 1. Current Gain Hfe vs. Base Width W_b for InGaAsP/InP HBT at different minority carrier diffusion lengths Lnb

Figure 2 shows the relationship between the minimum HBT switching speed t_{smin} under an optimal load ($t_s = 1/2(t_{on} + t_{off})$), base resistance R_b and collector capacitance C_c[1]. Figure 3 shows the relationship between the frequency response of a monolithic integrated InGaAsP/InP optical emitter consisting of four HBT's, and the HBT base resistance R_b; the relationship was derived with the SPICE program[10]. Obviously, R_b and C_c are the key parameters which determine the HBT speed and the frequency response of the entire circuit. In particular, R_b is especially important. From Figure 3 we can see that the frequency response of the OEIC drops 66 percent when R_b increases from 1 to 5 ohms.

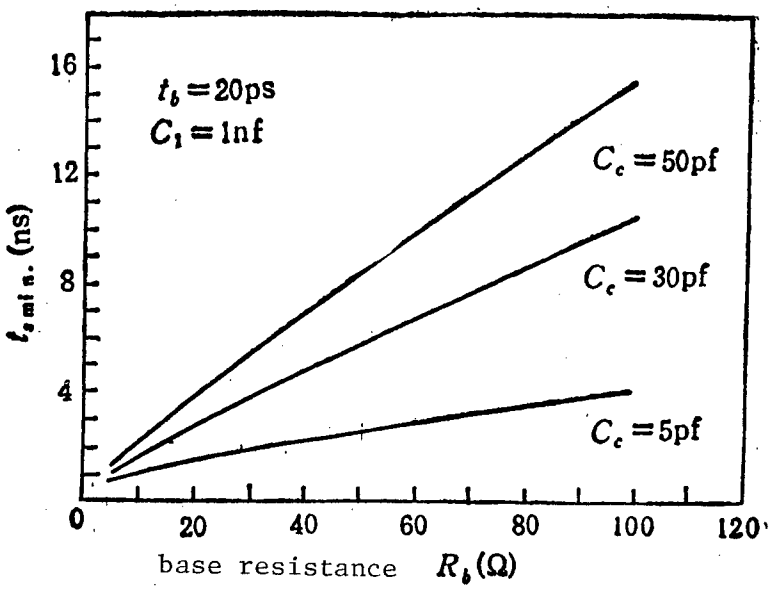

Figure 2. Relationship between minimum switching speed t_{smin} of InGaAsP/InP HBT and base resistance R at various collector capacitances C_c.

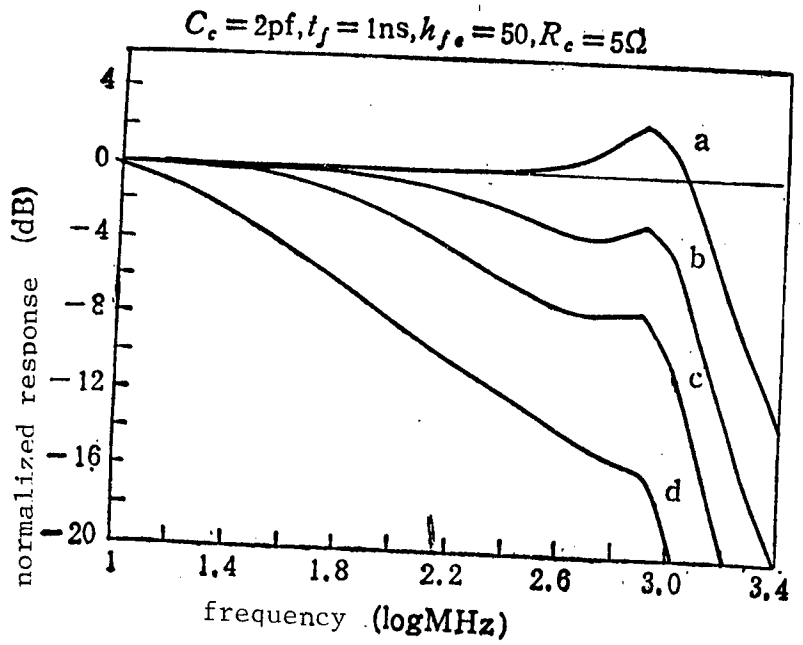

Figure 3. Frequency response of optical emitter comprised of four InGaAsP/InP HBT's Versus base resistance R_b of the HBT

In order to raise the gain and the speed of the device, we must reduce the base width, base resistance and collector capacitance. Nevertheless, it may not be possible to take care of all three parameters simultaneously; an overall consideration will have to be made when designing the device. To this end, we propose a quasi-planar HBT structure with a deep Zn diffusion outer base and two collectors, as shown in Figure 4. The advantages of this structure are: 1) the outer base is fabricated by diffusion to keep it as close to the inner base as possible, thus eliminating the problem of increasing base resistance with decreasing base width. 2) Two n^- -N collectors are used not only to reduce collector capacitance but also to avoid serious impact on the series resistance of the device in order to simultaneously improve speed and power. The presence of the two collectors can also reduce storage time[11] so that switching time can be raised. 3) It is essentially planar; this facilitates integration.

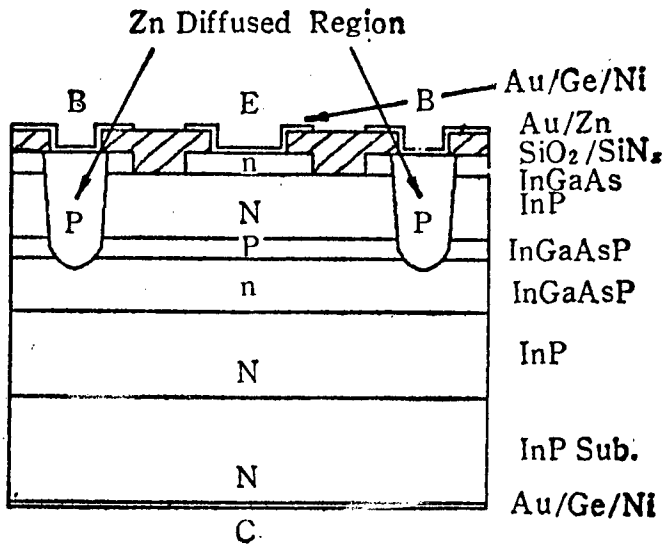

Figure 4. Structural Diagram of the Deep-Zn-Diffusion Outer Base, Quasi-Planar, Double-Collector InGaAsP/InP HBT

We also designed an OEIC consisting of an HPT [heterojunction photo transistor], HBT and LD [laser diode] (or LED [light emitting diode]), as shown in Figure 5. In this OEIC the optical emitter and other electronic devices are compatible longitudinally in structure. In order to take into account the characteristics of various devices, the structural parameters should be adjusted accordingly.

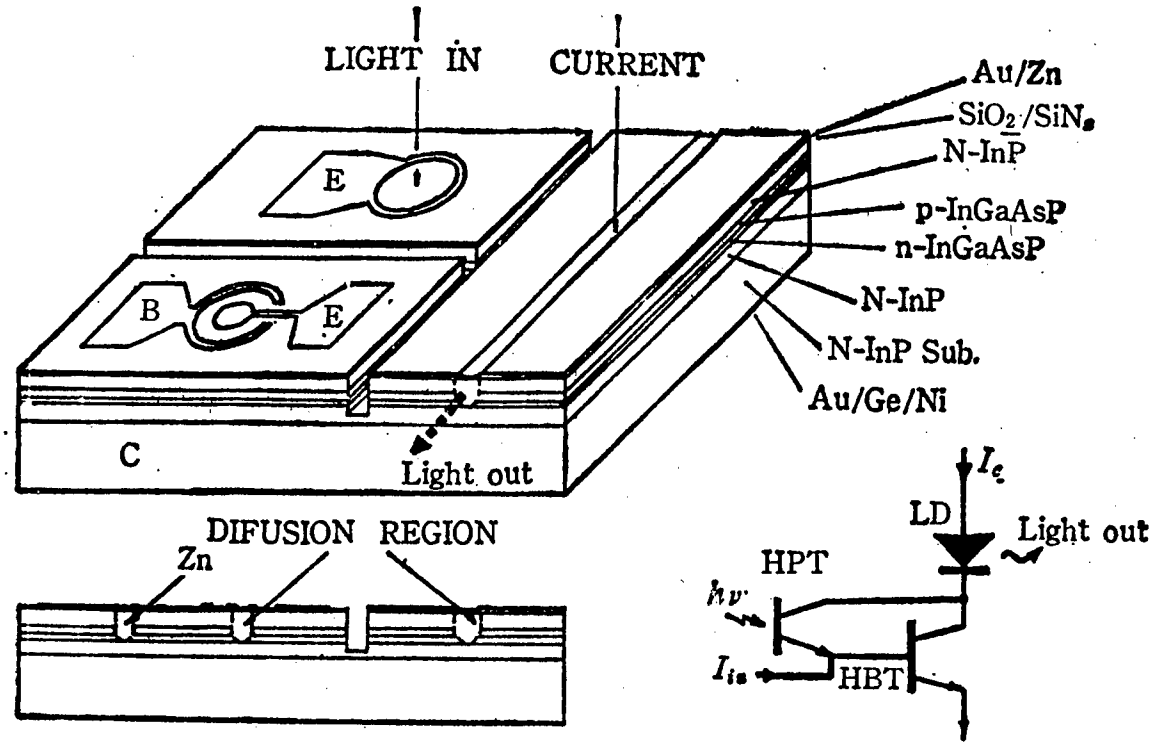

Figure 5. Structural diagram of an OEIC consisting of HPT, HBT and light-emitting device

II. Device Fabrication

The device uses a five-layer hetero-epitaxial material prepared by liquid phase epitaxy (LPE). The composition, dopant type and thickness of each layer are listed in Table 1. The dopant concentration for each layer is determined based on the design requirement for the device. In order to obtain a p^+-n^- type b-c junction, the dopant for p-type InGaAsP must have a low solid-phase-diffusion coefficient and low vapor pressure. The commonly used dopant Zn obviously cannot meet this requirement. We used Mn as the dopant and obtained better results. When p-type InGaAsP is doped at 10^{18} cm^{-3} and n-type material is not doped (n is approximately 1 x 10^{16} cm^{-3}), the epitaxial junction essentially coincides with the p-n junction.

Table 1. Structure of Epitaxial Material

epitaxial layer	composition	conducting type	dopant	thickness (μm)
cap layer	$In_{0.53}Ga_{0.47}As$	n	none	~0.5
emitter layer	InP	N	Te	~1.4
base layer	InGaAsP (λ_g = 1.3 μm)	p	Mn	~0.4
first collector	InGaAsP (λ_g = 1.3 μm)	n	none	~0.8
second collector	InP	N	Te	~5
substrate	InP	N	S	-

After completing the LPE process, the InGaAs layer other than the contact was selectively etched away with $H_2SO_4 : H_2O : H_2O$. It was followed by thorough rinsing. Thin films of SiO_2 and SiN_x were deposited on it by CVD [chemical vapor deposition] and PE-CVD [plasma enhanced chemical vapor deposition], respectively, as diffusion masks. The outer base was prepared by open-tube Zn diffusion[12].

Three types of composite metal are used as electrical contacts; Au/Zn in the p region, Au/Ge/Ni in the n region, and Ti/Au-Au at welding points on the dielectric film and on the connecting lines in the OEIC. After evaporation is done on these three composite metals, the device is alloyed in an N_2 atmosphere. Electrical testing and Auger microprobe analysis showed that 420°C is the optimal alloying temperature for InGaAs(P) with Au/Zn, Au/Ge/Ni and Ti/Au.

III. Device Performance and Discussion

1. Current Gain Hfe

Figure 6 [photograph not reproduced] shows the I-V characteristics of a typical device. We note two points: (1) Current gain Hfe increases as collector current rises when the injection is relatively low. Up until I_c = 10 mA, the trend between Hfe and I_c becomes unclear. (2) At I_c = 16 mA and V_{ce}= 5 V, Hfe = 22. This is close to the ideal Hfe for a device shown in Figure 1 with W_b of 0.4 μm and base dopant concentration of 10^{17} - 10^{18} cm^{-3}. These results indicate that the device fabricated only has a few recombination centers near the

heterojunction. Although some carriers injected from the emitter have been recombined and thus affected the gain of the device, because the number of recombination centers is not very large, the effect on gain was not very obvious at high implantation.

Figures 7(a) and 7(b) [photographs not reproduced] are the I-V characteristics of an abnormal device with emitter on the epitaxial face and on the substrate face, respectively. At the same collector current, Hfe is five times higher in the latter case. This anomaly indicates that the interface quality of the upper p-n junction is very different from that of the lower p-n junction. This may be attributed to the presence of more defects introduced by lattice mismatch at the InP/InGaAsP heterojunction interface. We did an X-ray bicrystal diffraction analysis on the epitaxial material used to fabricate this device. Figure 8 shows the oscillation curves. Curve a is the oscillation curve of four layers of epitaxial material (without InGaAs cap) and Curb b is the bicrystal diffraction oscillation curve of the material after we selectively etched the top InP layer. Obviously, there is considerable lattice mismatch at the InP layer interface. The mismatch between the lower three epitaxial layers with respect to their substrates is negligible. This proves our interpretation for the anomalous I-V behavior of the HBT. It also demonstrates the significance of material quality, especially interface quality, on the characteristics of an HBT.

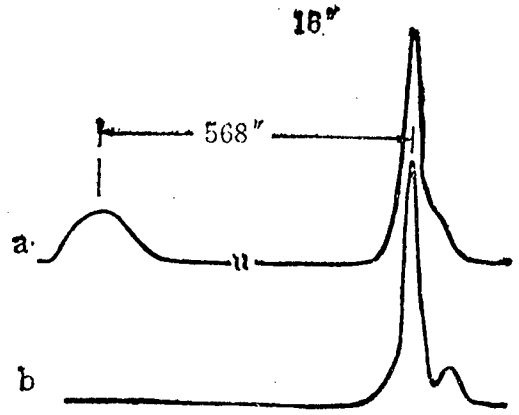

Figure 8. X-Ray bicrystal diffraction oscillation curves of the epitaxial material used to fabricate HBT showing anomalous I-V behavior; a. oscillation curve of the four-layer epitaxial material, b. oscillation curve of material with top InP layer etched away.

2. Offset Voltage (V_{offset}) of the Device and Its Symmetry

Figure 6 we can see that the offset voltage V_{offset} of the device is very low. More accurate measurements showed that the V_{offset} of most devices was less than 30 mV. This indicates that as long as the dual collector thickness could be properly controlled, the longitudinal symmetry of the device would not be seriously affected[13]. This gives the device a great deal of flexibility when it is used in an IC or OEIC.

3. Transient Characteristics and Optoelectronic Integration of the Device

Transient characteristics of the HBT are affected by longitudinal structural parameters such as carrier concentration distribution and layer thickness ratio. In order to obtain good transient response, we made an HBT with a 110-μm-diameter emitter using a 0.3-μm-thick $p = 1 \times 10^{13}\ cm^{-3}$ base and a 0.1-μm-thick $n = 6 \times 10^{15}\ cm^{-3}$ first collector. Upon irradiation by an 80-ps [picosecond] FWHM (full width half maximum) Gaussian light pulse ($\lambda = 1.3\ \mu m$) on its base with $V_{ce} = 2$ V, the electrical pulse response at the collector of the HBT was found to have a 300-ps rise time, as shown in Figure 9.

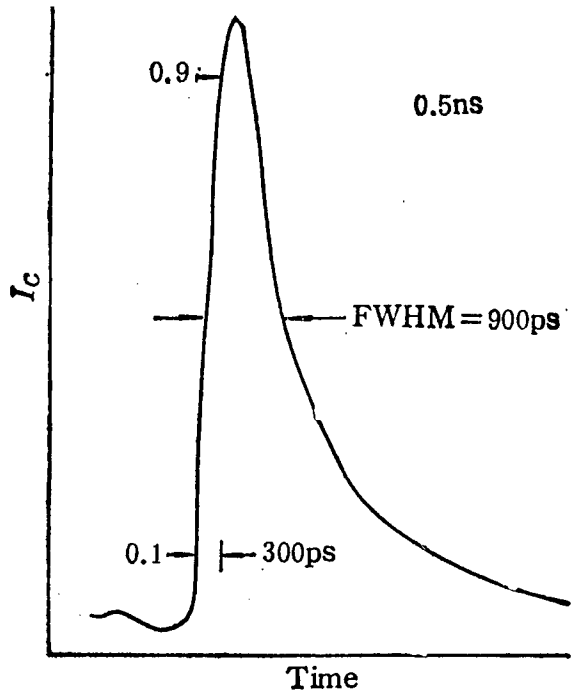

Figure 9. Transient collector current of the InGaAsP/InP HBT (base excitation light source is a Gaussian light pulse with FWHM = 80 ps)

Similar material was used to fabricate an OEIC as shown in Figure 5. The quantum efficiency was found to be low. We believe that this can be improved by properly reducing dopant concentration in the active region.

IV. Conclusions

The gain and frequency response of the InGaAsP/InP HBT and their relationship with the structural parameters of the device have been quantitatively analyzed in this paper. Based on this analysis, a quasi-planar structure and its fabrication techniques have been presented. The device designed was fabricated and its parameters were measured in order to analyze and discuss the relationship between its characteristics and material parameters and quality.

The authors wish to express their gratitude to Wang Chen [3769 2525] and Zhou Yingtong [0719 4481 0681] for their assistance, to Yan Zhixin [0917 1807 2450] of Shanghai University of Science & Technology for the beneficial discussion and to Chen Jingyi [7115 0079 0001] for his assistance in the X-ray bicrystal diffraction analysis.

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Fabrication of Submicron-Gate-Length Modulation Doped $Al_xGa_{1-x}As$/GaAs Field Effect Transistors

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[Article by Yang Yufen [2799 3768 5358] and Chen Zonggui [7115 1350 0964] of the Institute of Semiconductors, Chinese Academy of Sciences, and Zhang Ju [1728 4251] of the Department of Physics, Beijing Institute of Technology, manuscript received on 25 Jan 88: "Fabrication of Submicron-Gate Modulation Doped Field Effect Transistor (MODFET)"]

[Text] Abstract

The design principle of the material parameters of a modulation-doped field effect transistor (MODFET), the techniques for fabricating a 0.2-μm-gate-length T-type gate, and the conditions to obtain a 0.2-μm gate using electron beam (EB) lithography are described in this paper. Although the purity of the buffer-layer material is not sufficiently high (about 1×10^{15} cm^{-3}), because of the T-type structure, transconductance is 200 mS/mm [millisiemens per millimeter] at room temperature and 375 mS/mm at 77 K.

Key words: modulation doped, two-dimensional electron gas, submicron gate length, field effect transistor.

I. Introduction

Since the two-dimensional electron gas (TEG) was found to have excellent transport properties across a modulation-doped heterojunction, very rapid progress has been made in the past several years to develop high-speed and microwave devices based on it. The first AlGaAs/GaAs MODFET was fabricated in 1980[1]. Later, an inverted high-transconductance GaAs/AlGaAs MODFET was developed[2]. A single-quantum-well InGaAs/AlGaAs MODFET was successfully fabricated in 1985[3]. In a single-quantum-well structure, because the energy difference, ΔE_C, at the discontinuity point of the conduction band is relatively high, it is possible to reach a higher TEG density. A single-quantum-well double-heterojunction MODFET was also successfully fabricated in 1986[4]. The performance of

the device was significantly improved. As a low-noise amplifier (LNA), it is already used in the millimeter band. In 1986, Tasprit Singh et al.[5] suggested using an $(InAs)_m$ $(GaAs)_m$ superlattice in place of InGaAs to form the quantum-well channel: this would avoid the scattering caused by the potential fluctuation in the InGaAs channel due to "alloying." It was expected to significantly improve the performance of the device. However, this concept has not been experimentally confirmed.

Our research is limited to the AlGaAs/GaAs structure. The objective is to explore the feasibility of making an ultra-short T-type gate. If a gate length of less than 0.1 μm can be fabricated, we expect to see a new physical phenomenon. This is a worthwhile subject. The gate length we actually prepared is 0.2 μm. We will conduct further studies on ultra-short-gate-length structures on the order of 0.1 μm in the future.

II. Design Principle for Material Parameters

Modulation doped materials can be prepared by MBE [molecular beam epitaxy] or MOCVD [metallo-organic chemical vapor deposition]. In order to obtain a high-performance device, highest material purity is required. The physical principles determining the parameters of various layers of materials are given in the following.

1. High-Purity GaAs Buffer Layer

The primary function of this layer is to form a channel for the TEG. In order to lower the noise of the device and raise electron mobility, one needs to minimize the scattering of ionized impurities in this channel. To this end, this layer must be of the highest purity. Generally, dopant concentration should be below 10^{14} cm^{-3}. On the other hand, in order to reduce the parallel conductance associated with the buffer layer, it is more favorable to have p-type, rather than n-type, material. The appropriate thickness is 8000 A - 1 μm.

2. Undoped Insulating Layer

The electrons in the potential well near the heterojunction interface are not only subject to scattering by residual ionized impurities in the high-purity GaAs buffer layer, but also subject to Coulombic scattering of ionized impurities in the highly doped AlGaAs layer near the interface. As a result, electron mobility is reduced and noise is increased. In order to reduce the effect of Coulombic scattering, a high-purity undoped AlGaAs insulating layer of appropriate thickness is added between the buffer layer and the AlGaAs layer. The purpose is to increase the distance between the potential well and the highly doped AlGaAs layer to reduce the Coulombic effect of the electrons in the TEG due to ionized impurities; this raises electron mobility and lowers noise. However, the presence of this high-purity AlGaAs insulating layer would also lower the density of the TEG. Therefore, the thickness

of this layer must be properly chosen. Based on theoretical analysis and experimental results, we found that it is most appropriate to choose 30 Å.

3. Heavily Doped AlGaAs Layer

The thickness and concentration of the heavily doped AlGaAs layer are also important material parameters because they are closely related to the TEG density in the channel, noise characteristics and transconductance. For instance, in the short-channel approximation, the noise index is[6]:

$$F = 1+2\pi K_f C_{GS}\sqrt{(R_s + R_g)/g_m} \quad (1)$$

Since

$$g_m = C_{GS}/L_G \quad (2)$$

$$C_{GS} = L_G Z/d_d \quad (3)$$

we have

$$F = 1 + 2\pi K_f f \sqrt{\varepsilon Z L (R_s + R_g)/d_d v_s} \quad (4)$$

where f is the working frequency; K_f is a fitting factor (ranging from 1.5 - 2.0); R_s and R_g are source and drain resistance, respectively; ε is the dielectric constant; d_d is the thickness of the AlGaAs layer; Z and L are the length and width of the channel, respectively; and v_s is the saturated drift velocity of an electron. When other parameters are fixed, this equation shows that an increase in the thickness d_d of the AlGaAs layer will lower the noise index. As a matter of fact, if the thickness of the AlGaAs layer is increased by too much, the gate bias cannot possibly deplete the region below the gate channel in operation. Consequently, there is an electrically neutral zone which forms a deleterious parallel conductance. In addition, it also causes the ratio of gate length to channel thickness to drop. The ultimate effect is the lowering of transconductance and deterioration of performance. Thus, the principle governing the determination of the thickness of the AlGaAs layer is to ensure that there is not a charge-neutral zone in the deice during operation. When f_T is 40 GHz, K = 1.5, intrinsic transductance must exceed 400 mS/mm, and gate length is 0.5 μm, based on equations (1)-(4), the thickness of the AlGaAs layer should be approximately 400 Å.

Dopant concentration is determined by two factors. It not only must ensure formation of a high-quality Schottky barrier on the AlGaAs surface, but also must minimize the density of "DX" center traps to guarantee sufficient TEG density. It was experimentally demonstrated that the suitable value is $2 - 3 \times 10^{18}$ cm^{-3}.

4. Heavily Doped GaAs Surface Layer

This layer serves two functions. One is that the presence of a heavily doped GaAs surface layer facilitates the fabrication of a high-quality ohmic contact. The other is it protects the AlGaAs layer from any detrimental chemical changes. Based on these two aspects, it was determined that a 200-300-A-thick layer is sufficient. Based on these considerations, the material parameters chosen can be summarized as shown in Figure 1.

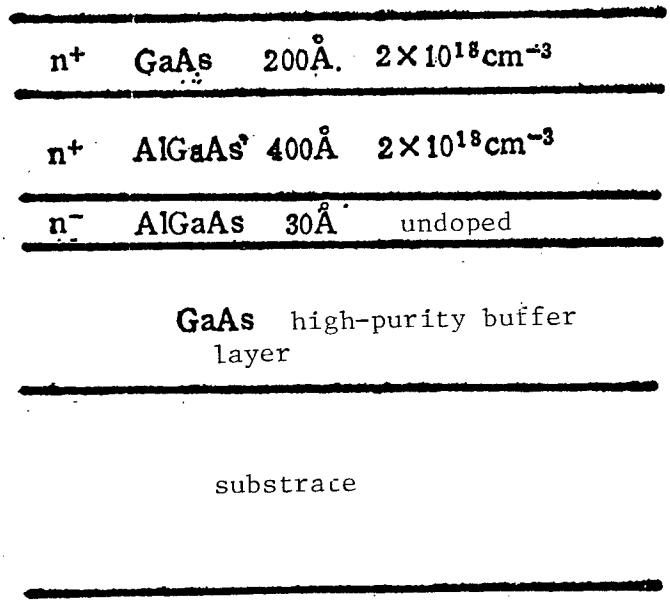


Figure 1. MODFET material parameters

III. Fabrication Techniques

The fabrication techniques for a MODFET are similar to those for a MESFET [metal semiconductor field effect transistor]. Because we are developing an ultra-short T-type gate structure, unique procedures are used to fabricate the gate. A detailed explanation of the techniques is given below.

(1) Mesa Formation

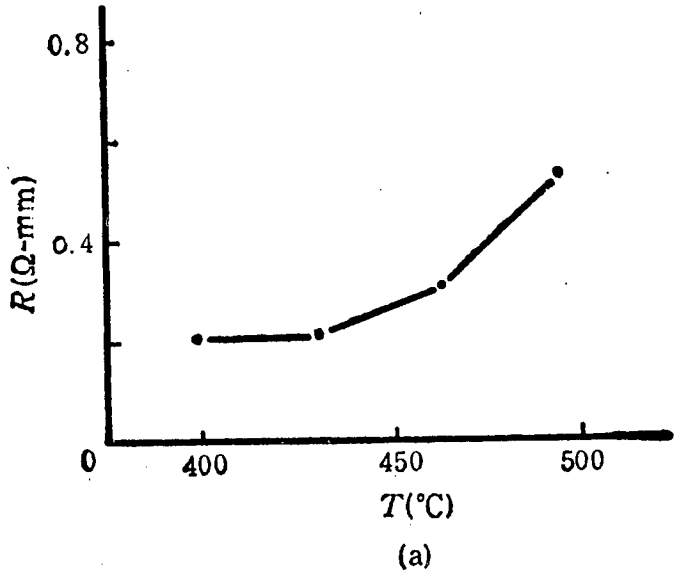
The key in this step is to control the mesa height and to choose an isotropic etching solution in order to ensure that the gate does not break off at the slope. It was found that the H_3PO_4:H_2O_2:H_2O system is more desirable because it could form trapezoidal structures on all four sides. The height of the mesa should exceed the distance between the

TEG potential well, and the surface. Based on the material parameters chosen, it ought to be 1500 to 2000 Å. Excessive mesa height will make gate fabrication difficult.

(2) Ohmic Contacts for Source and Drain

In order to successively strip the metal to form a perfect ohmic contact pattern, it is necessary to use a photoresist. After exposing to light, the photoresist must be immersed in chlorobenzene for a suitable period of time. This amount of time needs to be empirically determined based on the chemicals used and on the laboratory environment.

In order to achieve good ohmic contact (less than 0.2 Ω·mm), factors such as materials, layer thickness, and alloying temperature and time cannot be ignored. The researcher has to find the optimal experimental conditions based on his equipment and type of alloying furnace. We chose to use the AuGa-Ni-Au system at 2000 Å - 500 Å - 1000 Å thickness, respectively. The alloying temperature is 430 ℃, time is 90 seconds, and the ohmic contact is 0.15-0.18Ω·mm. Figures 2(a) and 2(b) show the dependence of contact resistance upon alloying temperature for a typical ohmic contact and the ohmic contact pattern, respectively.



(a)

Figure 2(a). Ohmic contact resistance versus alloying temperature

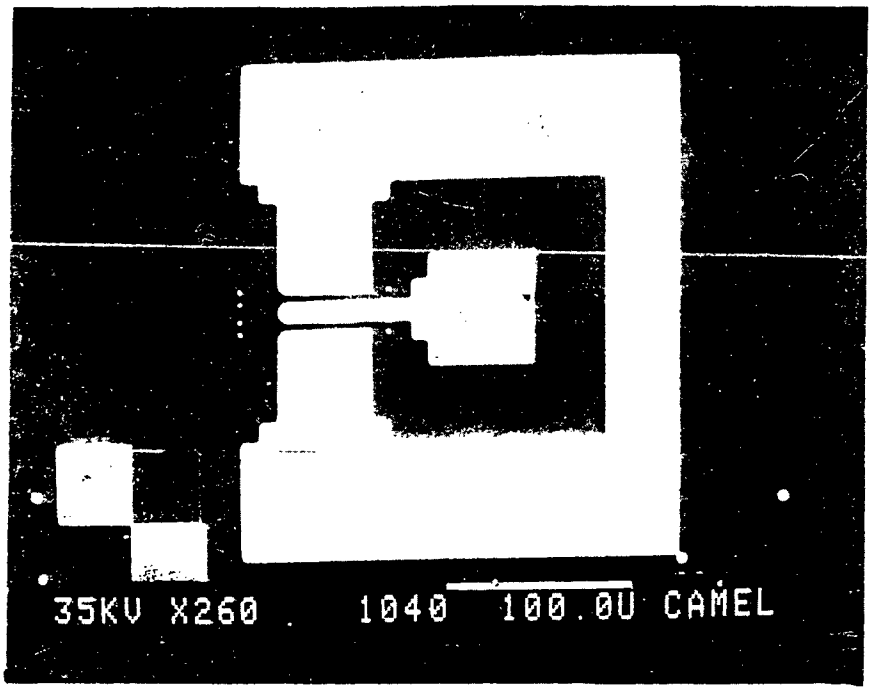


Figure 2(b). Picture of source-drain ohmic contact

(3) Fabrication of Ultra-Short T-Type Gate

In order to fabricate an ultra-short T-type gate, we employed a triple-layer EB lithographic technique; i.e. PMMA [polymethyl methacrylate]-copolymer-PMMA. The thickness of each layer, the EB lithographic conditions and the developing time for each layer after exposure must be carefully controlled. When the EB current was held at 0.0170 nA [nanoampere], a gate length of 0.2 μm could be obtained.

Before evaporating the gate metal, extreme care had to be taken to etch the gate groove. The drain current was simultaneously monitored. Etching was immediately stopped after reaching the specified range. In order to minimize surface contamination to ensure that a high-quality Schottky barrier could be obtained, it was found that $NH_4OH:H_2O_2:H_2O$ is the preferred etchant. Prior to gate metal evaporation, the surface was cleaned with $NH_4OH:H_2O$. The thickness of the gate metal could be controlled at 4000 Å to 5000 Å. At the same thickness, the gate resistance of a T-type gate is less than 1/2 that of a conventional gate. The typical structure of a 0.2-μm gate is shown in Figure 3.

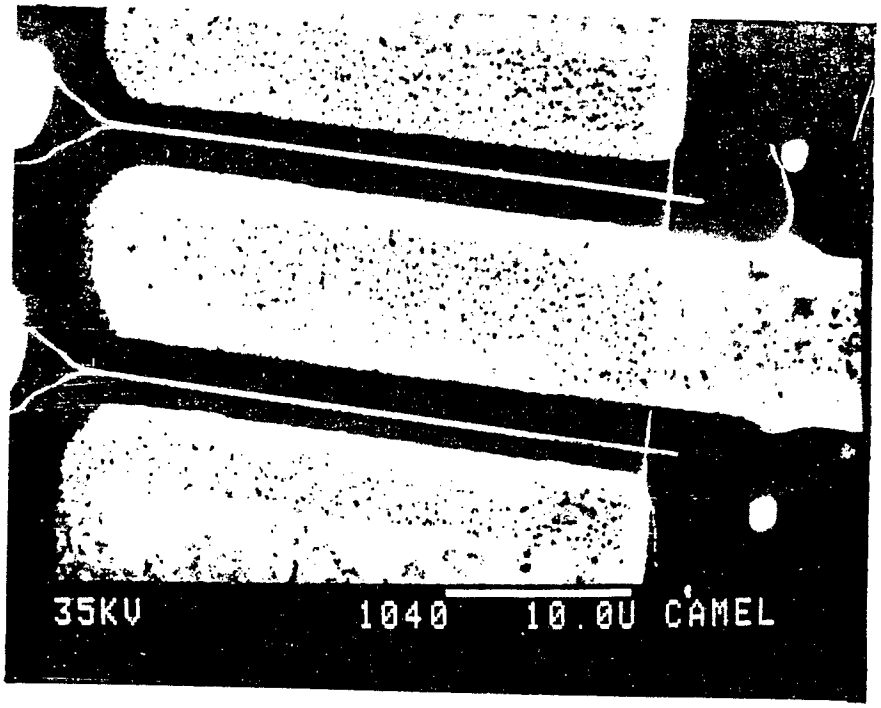


Figure 3. Structure of Gate With 0.2-μm Gate Length

In order to facilitate the bonding of conductive leads, the device was metallized once more after the Schottky barrier was formed. The thickness of the evaporated gold is between 1500 Å to 2000 Å. It was then followed by dielectric protection and trimming.

IV. Conclusions

Figure 4 [photograph not reproduced] shows the room-temperature drain current-voltage characteristics of a device whose gate is 0.2 μm long, 2 x 50 μm wide. The curve shows excellent saturation and pinch-off characteristics. The g_m-V_{GS} transconductance curves are shown in Figure 5. These curves were provided by the HP 4145 semiconductor parametric analyzer. The room-temperature transconductance is approximately 200 mS/mm and the maximum is 240 mS/mm. Figure 6 shows the I_D-V_{GS} transition characteristics. When the drain voltage is 1 volt, the pinch-off voltage is 1.8 volts. The channel resistance R_t-V_{GS} characteristics are shown in Figure 7. Figure 8 shows the I_D-V_D curves of a device at room temperature and at liquid-nitrogen temperature. The transconductance of the device whose transconductance is 200 mS/mm at room temperature is 375 mS/mm at liquid-nitrogen temperature.

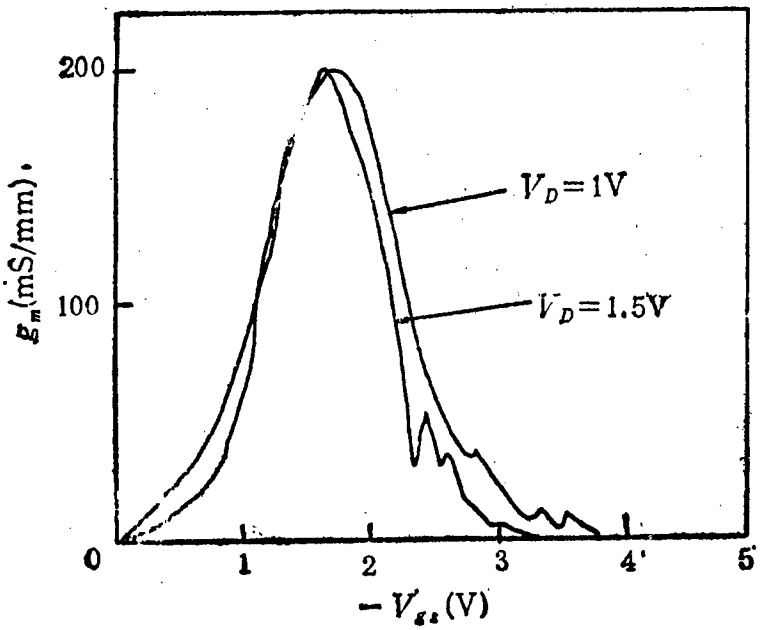


Figure 5. Transconductance g_m-V_{GS} Characteristic Curves

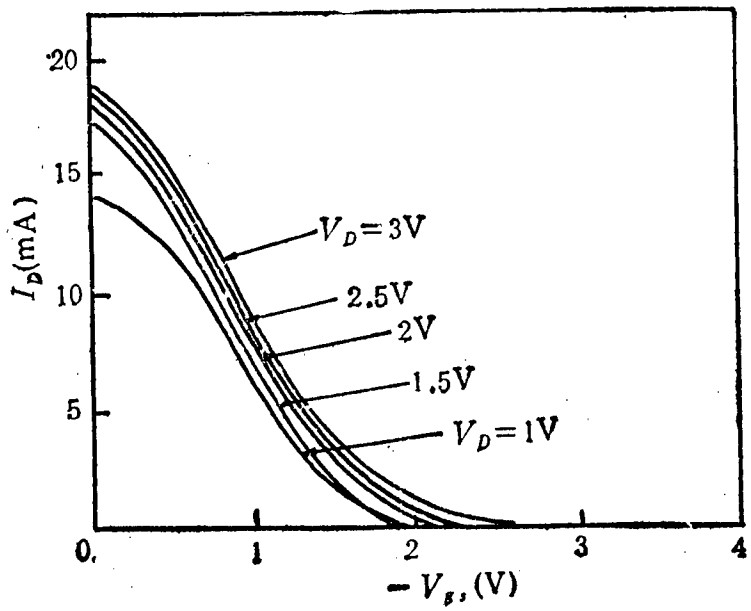


Figure 6. I_D-V_{GS} Transition Characteristic Curves

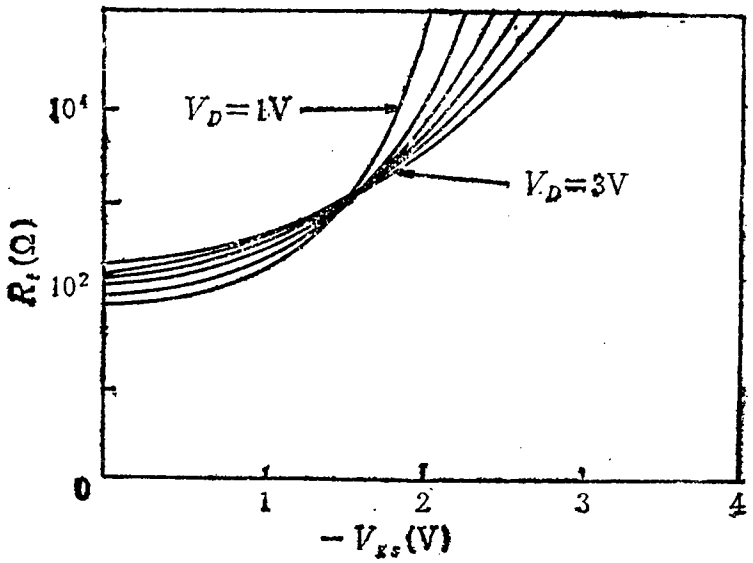
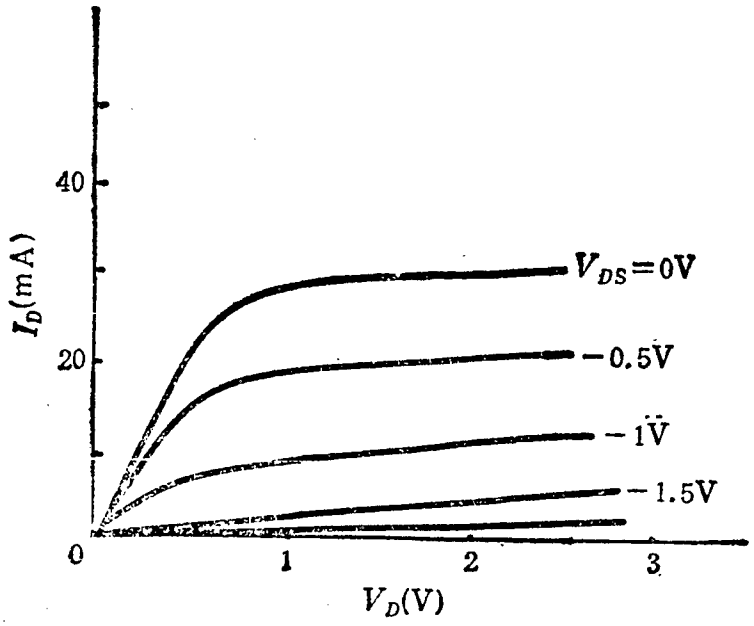


Figure 7. Variation of Channel Resistance R_t-V_{GS}



(a)

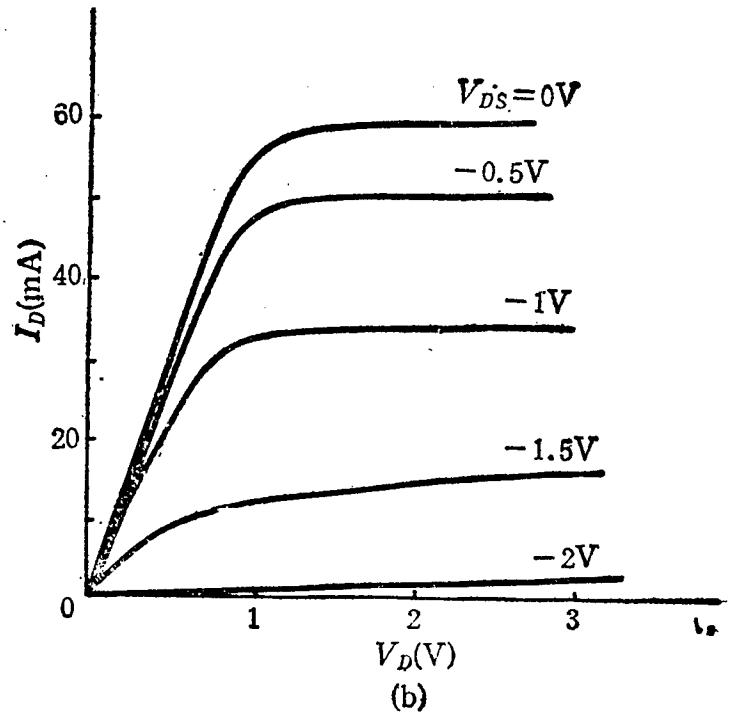


Figure 8. I_D-V_D at (a) room temperature (b) liquid-nitrogen temperature

It was discovered that the quality of materials is inconsistent transversely. In most cases, only a portion of the material can be used to make devices with good characteristics. There are two major parameters affecting the quality of the material; both electron mobility and TEG concentration must have appropriate values. It is not possible to fabricate a good device with one parameter high and the other low. Usually, it is required that electron mobility should be above 80000 $cm^2/v.s$ [volt-second] and TEG density should reach 8×10^{11} cm^{-2} at liquid-nitrogen temperature. In gate fabrication, it was also found that a Schottky barrier prepared by thermal evaporation is better than one made by EB evaporation. Our experience shows the rate of evaporation should not be too high. 6 - 8 Å per second seems to be appropriate. The gate resistance using the three-layer fabrication technique is apparently lower than that obtained using a two-layer technique. Experimentally, the fabrication of T-type gates is feasible. The T-type gate structure is necessary, especially for ultra-short gate devices.

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Transient Annealing of As^+, Si^+ Dually Implanted Si GaAs

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[Article by Fan Weidong [5400 0251 2767] and Wang Weiyuan [3769 3262 3293] of the Shanghai Institute of Metallurgy, Chinese Academy of Sciences, manuscript received on 5 Dec 87: "Transient Annealing Behavior of As^+, Si^+ Dually Implanted GaAs"]

[Text]

Abstract

The effect of As^+ implantation of the Si^+-implanted active layer in As^+, Si^+ dually implanted SI GaAs is studied at different energy and dose levels. First, the activation efficiency and carrier mobility of the active layer of a dually implanted specimen after transient annealing and the channel spectra of the material before and after annealing are presented. Our experimental results showed that the As^+, Si^+ dually implanted specimen could activate Si^+ at a lower annealing temperature compared to that of a Si^+-implanted specimen. A high-performance active layer can be obtained at a suitable high temperature.

Key words: As^+, Si^+ dual implantation; SI GaAs; transient annealing; activation efficiency; mobility.

I. Introduction

Si^+ implantation is used to dope the active layer in a GaAs MESFET [metal semiconductor field effect transistor]. The conventional annealing technique for ion implantation would cause the redistribution of impurities in the substrate and implanted ions; this creates a carrier distribution tail and lowers the activation efficiency of the implanted ions. To this end, high-temperature transient annealing has been widely studied in recent years[1]. The characteristics of the active layer have significantly improved with transient annealing; however, its mobility is relatively low[2]. This study was therefore initiated.

II. Experiment and Results

Refer to reference [2] for details regarding samples. Implantation deviation angle and annealing conditions used in the experimental work. For Si^+ implantation, energy E_{Si} = 150 KeV and dose ϕ_{Si} 2 x 10^{13} cm^{-2}. Different energy and dose levels were used for As^+ implantation. The annealing time was 6 seconds for all cases. Mesa technology was used to form van der Pauw patterns to measure the activation efficiency η and mobility μ of the active layer. Back-scattering channel spectrometry was used to measure the minimum channel productivity χ_{min}.

Figure 1 shows the dependence of the Si^+ activation efficiency η and the active-layer mobility μ upon annealing temperature for an annealed As^+, Si^+ dually implanted specimen (E_{As} - 100 KeV, ϕ_{As} = 1 x 10^{13}, 1 x 10^{14} or 1 x 10^{15} cm^{-2} for As^+ implantation) and Si+ singly implanted specimen. With the ϕ_{As} = 1 x 10^{13} cm^{-2} specimen, the values of μ were 60 and 75 percent and the corresponding values of η were 3500 and 2700 $cm^2/v.s$ when annealed at 1050 and 1100°C, respectively. They were all higher than those of the Si^+ singly implanted specimen. η begins to decrease when ϕ_{As} is further increased.

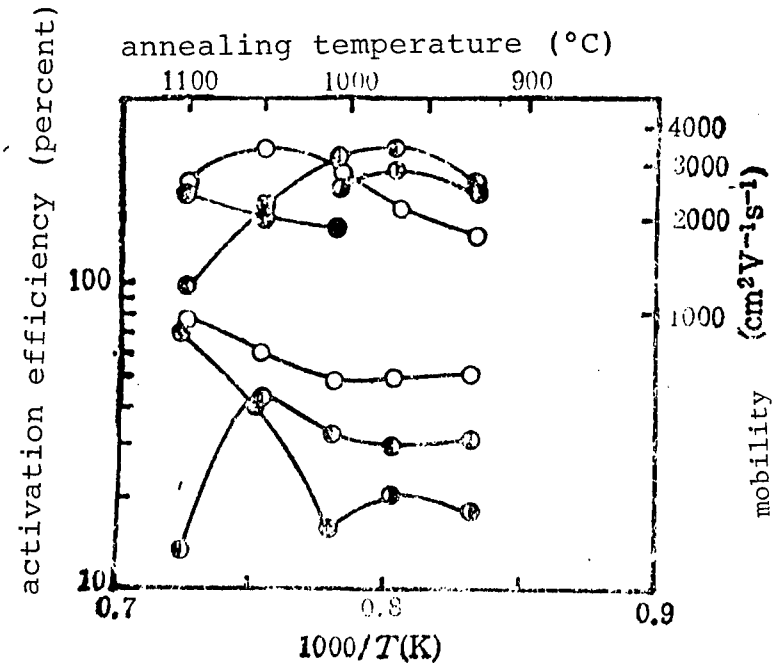

Figure 1. Dependence of Si^+ activation efficiency and active layer mobility upon transient annealing temperature (annealing time 6 seconds) for As^+, Si^+ dually implanted and Si^+ singly implanted specimens. E_{As} = 100 KeV

o ϕ_{As} = 1 x 10^{13} cm^{-2}, • ϕ_{As} = 1 x 10^{14} cm^{-2}, ⌀ ϕ_{As} = 1 x 10^{15} cm^{-2}, ● ϕ_{As} = 0

Figure 2 is a comparison of two dually implanted specimens at two energy levels. We can see that η depends on E_{As}. Lower E_{As} corresponds to higher η. At 1010 C - 1050°C, η > 80 percent and μ is about 1700 $cm^2/v.s$. In Si^+ singly implanted specimens annealed at 1010, 1050, and 1100°C, the values of η are 15, 40 and 70 percent, respectively. They are significantly lower than those of dually implanted specimens (the values of μ are 1900, 2020 and 2400 $cm^2/v.s$). Summarizing the results in Figures 1 and 2, at a lower annealing temperature, the As^+, Si^+ dually implanted sample has higher η and μ compared to those of a Si^+ singly implanted sample. Furthermore, its characteristics are dependent upon E_{As} and ϕ_{As}.

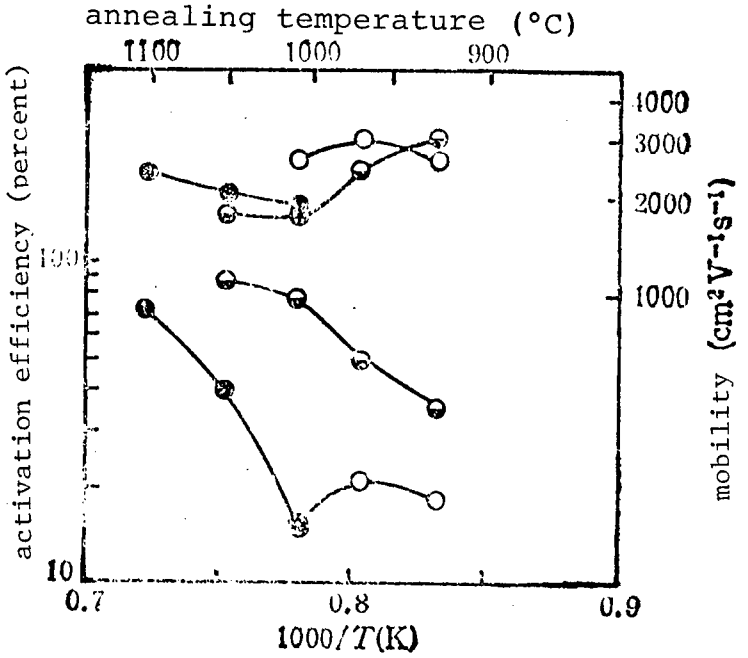

Figure 2. Dependence of Si^+ activation efficiency and active layer mobility upon transient annealing temperature (annealing time 6 seconds) for As^+, Si^+ dually implanted and Si^+ singly implanted specimens.

- ● E_{As} = 50 KeV, $\phi_{As} = 1 \times 10^{15}$ cm^{-2}
- o E_{As} = 100 KeV, $\phi_{As} = 1 \times 10^{15}$ cm^{-2}
- ● E_{As} = 0, ϕ_{As} = 0.

Figure 3 shows the back-scattering channel spectra of the dually implanted specimen before and after transient annealing. The channel spectrum of the unimplanted zone essentially coincides with that of the annealed implanted zone. The values of χ_{min} were experimentally calculated to be 6.0, 77.4 and 5.3 (or 5.4) percent in the unimplanted zone, in the implanted zone prior to annealing, and in the implanted zone after annealing at 920°C (or 1050°C), respectively.

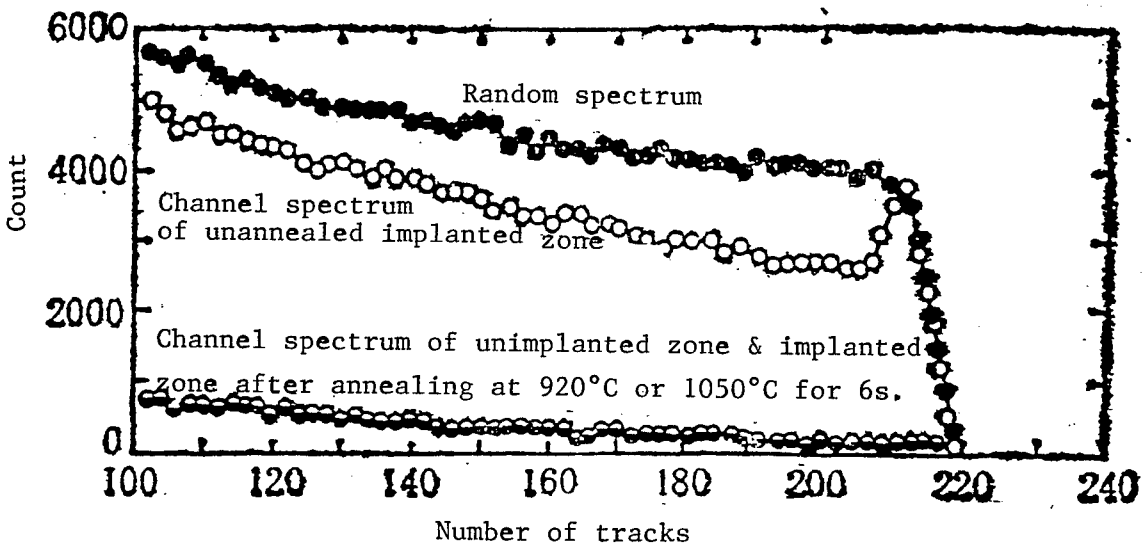

Figure 3. Back-scattering spectra (He^+, 2 MeV) of the As^+, Si^+ dually implanted specimen (E_{As} = 100 KeV, ϕ_{As} = 1 x 10^{15} cm^{-2}) before and after transient annealing.

III. Discussion

Solid phase epitaxy to repair damage from ion implantation has two mechanisms[3]. One is to grow epitaxially from the surface to the implanted layer and the other is to grow from the perfect region on the substrate toward the implanted layer. Studies[3] have shown that the second type of solid phase epitaxy will take place when the implantation dose is too small to cause any surface damage. If implantation causes any surface damage, the first type of epitaxy will occur. In this experiment, because the surface was damaged as a result of As^+ implantation in the preparation of the As^+, Si^+ dually implanted specimen, the first type of solid phase epitaxy occurred during annealing. The annealing of the Si^+ singly implanted specimen will undergo the second type of solid phase epitaxy. Because surface atoms have higher energy, upon activation by certain external energy, surface defects are first healed or eliminated. The precipitate released can further heal the defects in inner layers. Hence, the first mechanism occurs at a lower temperature. Therefore, the defects in a dually implanted specimen can be eliminated at a lower transient annealing temperature. It behaves as an active layer with a certain implanted ion activation and mobility.

The mobility of a Si^+ singly implanted specimen is lower than that a As^+, Si^+ dually implanted specimen. Its quality is also poorer. It si proposed that this is due to the volatilization of As during annealing on the surface which becomes a diffusion scattering source[4].

Consequently, the mobility of the surface layer is lower. In the dually implanted specimen, the surface is stabilized by As^+ implantation to weaken the above effect. The fact that a dually implanted specimen has a lower χ_{min} is another piece of evidence of high surface quality.

In order to obtain a high-quality active layer, we should consider the energy and dose of As^+ implantation as a whole. Based on this work, the optimal conditions are $E_{As} < 100$ KeV and $\phi_{As} < 1 \times 10^{13}$ cm^{-2}.

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Si^+, Mg^+ (Buried Layer) Double Implanted GaAs MESFET

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[Article by Ou Haijiang [2962 3189 3984], Wang Weiyuan [3769 3262 3293], Zhao Qihua [6392 1505 5478], and Jiang Xinyuan [5592 2450 0337] of Shanghai Institute of Metallurgy, Chinese Academy of Sciences, manuscript received on 11 Dec 87: "Si^+, Mg^+ (Buried Layer) Double Implanted GaAs MESFET"]

[Text] Abstract

The characteristics of an Si^+-implanted and Si^+, Mg^+-(buried layer)-double-implanted GaAs MESFET [metal semiconductor field effect transistor] have been compared. Experimental results showed that the effect of substrate impurities on the active layer could be greatly reduced by putting down a high-energy-implanted Mg^+ (buried) layer. It is easier to produce better GaAs E- and D-MESFET's than Si^+ single implantation. In addition, the uniformity of the threshold voltage V_{th} is improved.

I. Introduction

One of the primary causes for the low yield of GaAs IC's is the uniformity of high-temperature annealed ion-implanted SI GaAs.[1] In recent years, a GaAs MESFET with a Be^+ buried layer and an oscillator ring made of this material have been reported.[2,3] We believe that Mg^+ can achieve the same effect. Based on an in-depth study of the electrical characteristics of high-energy-Mg^+-implanted and Si^+, Mg^+-doubly-implanted materials, details on the Si^+, Mg^+ double implantation FET are here reported.

II. Si^+, Mg^+ Double Implantation

Experimentally, LEC[100] [liquid encapsulated Czochralski] In-doped SI GaAs single crystal was used as the substrate. $^{28}Si^+$ and $^{24}Mg^+$ were implanted 7° off [100]. Afterward, it was annealed at 800°C in an N_2 and H_2 atmosphere for 30 minutes.

Figure 1 shows the comparison of carrier concentration distribution of SI GaAs doubly implanted with Si^+ and Mg^+ to that only singly implanted with Si^+ and Mg^+. The buried p-type layer helps eliminate the tail in the electron concentration with Si^+ single implantation. Furthermore, under the proper conditions for Si^+, Mg^+ double implantation, it is possible to form a very steep p^+-n junction in the substrate.

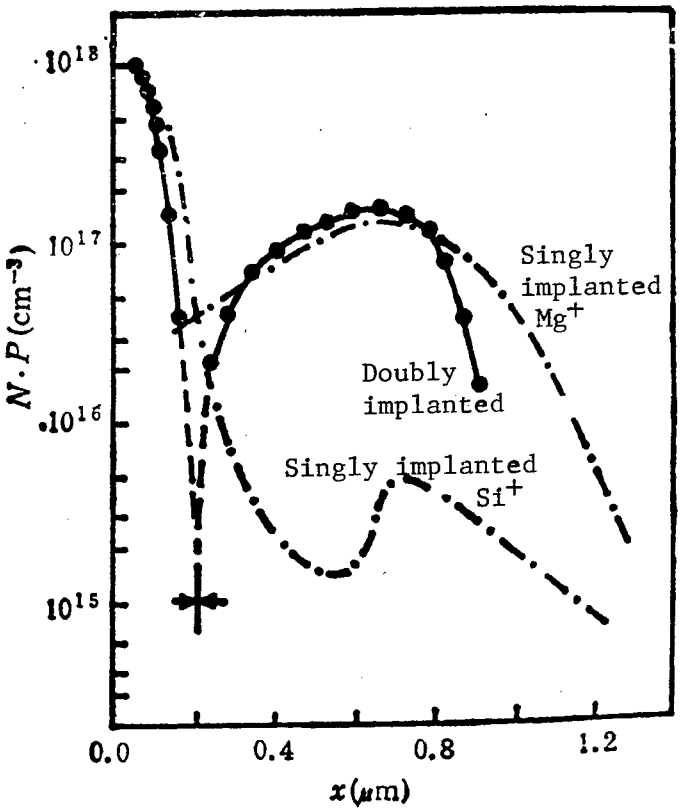

Figure 1. Carrier Concentration Distribution of Si^+, Mg^+ Double Implantation (Compared to Single Implantation), 800°C, 30-min Annealing
Si^+: 60 keV, 2×10^{13} cm^{-2} Mg^+: 600 keV, 8×10^{12} cm^{-2}

III. GaAs MESFET with Buried Mg Layer

When the amount of Mg^+ implanted is not too different from that of Si^+, the net donor concentration distribution in the implantation layer can be approximately expressed as:

$$N(x) = N_{max} \exp\left(-\frac{(x-R_1)^2}{2\sigma_1^2}\right) - P_{max} \exp\left(-\frac{(x-R_2)^2}{2\sigma_2^2}\right) \qquad (1)$$

where N_{max} and P_{max} can be approximated by the measured peak electron and hole concentrations with single implantation of Si^+ and Mg^+, respectively. R_1, R_2, σ_1 and σ_2 are the corresponding Gaussian distribution parameters. They are not the same as theoretical LSS range parameters and are experimentally determined.

Let us assume that the space charge layer on either side of the p-n junction can be approximated by depletion theory. Then, the positions of the depletion layers, x_n and x_p with respect to the surface, can be determined by the following equations:

$$\begin{cases} \frac{q}{\varepsilon}\int_{x_n}^{x_p} N(x)(x_j - x)dx = \frac{kT}{q}\ln\frac{|N(x_n)N(x_p)|}{n_i^2} \\ \int_{x_n}^{x_p} N(x)dx = 0 \end{cases} \tag{2}$$

where q is the electronic charge, ε is the absolute electrical capacitance coefficient of GaAs, k is Boltzmann's constant, and n_i is the intrinsic carrier concentration of GaAs. The pinch-off voltage is defined as:

$$V_p = -\frac{q}{\varepsilon}\int_0^{x_n} xN(x)dx \tag{3}$$

and the effective channel thickness d and effective dopant concentration N_d are:

$$d = 2\varepsilon V_p/(qN_s) \tag{4}$$

$$N_d = N_s/d \tag{5}$$

Here,

$$N_s = \int_0^{x_n} N(x)dx$$

Thus, the I-V [current-voltage] characteristics of the device can be calculated based on a two-zone model. When a channel is carved, the channel depth is t. Then, R_1-t and R_2-t are used to replace R_1 and R_2 in the above equations.

The gate length of the MESFET is L_g=1 μm. Other parameters such as the source-drain distance, gate width, and conditions for Si^+, Mg^+ double implantation will be explained in experimental results.

Figure 2 shows the dc output of a GaAs D-MESFET with a buried Mg layer. The solid curves represent experimental results. At V_g = 0.5 V, the maximum transconductance g_m=220 ms/mm. It is obviously better than the best device prepared by Si^+ single implantation (i.e. g_m=150 ms/mm). The dotted curves are I-V lines calculated based on the two-zone model using the approximation equations for effective dopant concentration and effective channel thickness (i.e. equations (4) and (5)). The parameters used in the computation are: source series resistance R_s (Ω)=25Ω, drain series resistance R_d=130Ω, channel depth t=0.035 μm, mobility μ_n=3400 $cm^2/V\cdot s$, critical electric field E_c=3530 V/cm, gate length L_g=1 μm, gate width W=30 μm, built-in field V_{b1}=0.7 V, intrinsic carrier concentration n_i=1.10^7 cm^{-3}.

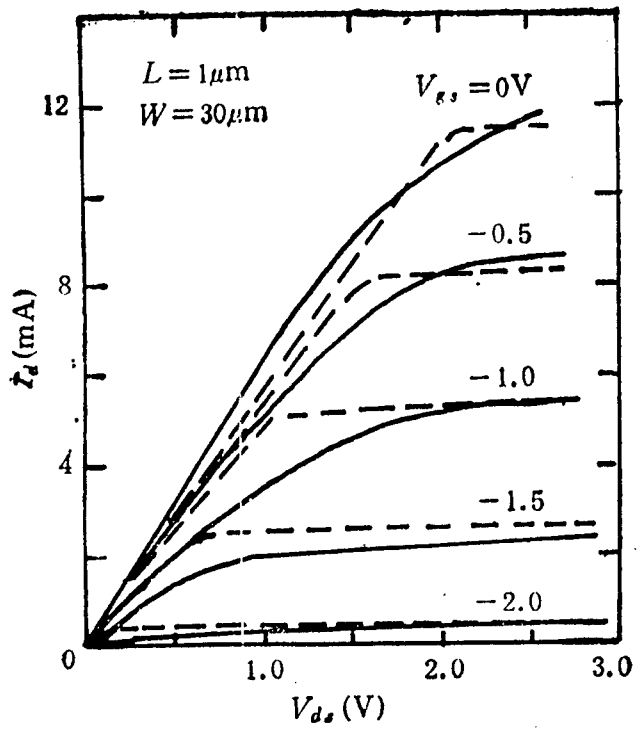

Figure 2. Output I-V Characteristics of GaAs D-MESFET with Buried Mg Layer (implantation and device preparation conditions: Si^+, 60 keV, $2x10^{13}$ cm^{-2}; Mg^+, 550 keV, $5x10^{12}$ cm^{-2}, channel depth 350 Å)

Figure 3 shows the characteristics of a GaAs E-MESFET with a buried Mg layer at V_{th}=0. It was found experimentally that it would be easier to produce an E-MESFET after laying down an Mg layer.

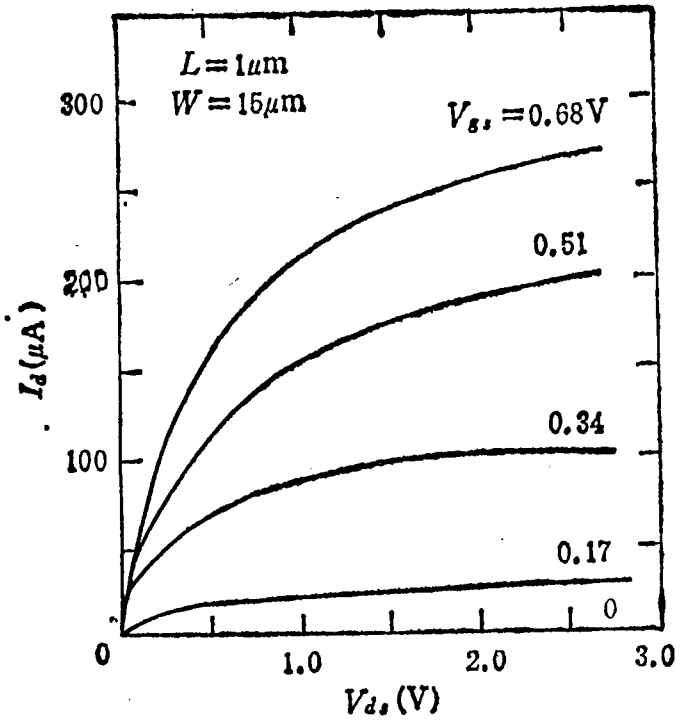

Figure 3. Output I-V Characteristics of GaAs E-MESFET with Buried Mg Layer (implantation and device preparation conditions: Si^+, 150 keV, $8x10^{12}$ cm^{-2}; Mg^+, 400 keV, $5x10^{13}$ cm^{-2}, through 400 Å, Si_3N_4)

Table 1 compares the results of V_{th} measured with a GaAs MESFET prepared on a 1.5 x 2 cm SI GaAs substrate with a buried Mg layer to that of a conventional (without a buried Mg layer) GaAs MESFET. A total of 1156 devices were measured. The table shows that the uniformity of V_{th} is improved by 27 percent after laying down a buried Mg layer (V_{th} changes from -1.36 V to -0.59 V because the n-type active layer is thinner).

Table 1. Comparison of V_{th} for GaAs MESFET with and without Mg Buried Layer (L_{sd} = 10 μm, W = 20, 40, 160, 320 μm)

Type	implantation condition			V_{th} (V)	δV_{th} (mV)	$\frac{\delta V_{th}}{(V_{th}-0.7V)}$
	ion	E(keV)	$\phi(cm^{-2})$			
w/o layer	Si^+	60	$6x10^{12}$	-1.36	173	8.4%
with layer	Si^+	60	$6x10^{12}$	-0.59	78	6.1%
	Mg^+	550	$1.2x10^{13}$	-0.59	78	6.1%

IV. Discussion

Since the Mg buried layer can eliminate the effect of non-uniform impurities on the n-type active layer, the double implantation of Si^+ and Mg^+ can improve the uniformity of V_{th}. Moreover, it is easier to produce an E-MESFET. In addition, double implantation can make surface and bulk electron concentration distribution steeper to raise electron peak concentration to increase transconductance. If the gate length can be further reduced, and a self-alignment technique is used, then high performance E- and D-MESFET's can be produced. The effect of the p-n junction beneath the active layer on its high frequency performance is still yet to be discussed.

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Photoluminescence Studies of $In_xGa_{1-x}As/GaAs$ Strained Single Quantum Well Structures Under Hydrostatic Pressure

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[Article by Li Guohua [2621 0948 5478], Zheng Baozhen [6774 1405 4176], Han Hexiang [7281 0735 4161] and Wang Zhaoping [3076 0340 1627] of the Institute of Semiconductors, Chinese Academy of Sciences, and T. G. Andersson and Z. G. Chen of the Department of Physics, Chalmers University of Technology, Goteborg, Sweden, manuscript received on6 Oct 88, supported by the National Natural Science Foundation: "Photoluminescence Studies of $In_xGa_{1-x}As/GaAs$ Strained Single Quantum Well Structures Under Hydrostatic Pressure"]

[Text] Abstract

Photoluminescence studies of $In_xGa_{1-x}As/GaAs$ strained single quantum well (SSQW) structures under static pressure have been performed at room and liquid-nitrogen temperatures under static pressure of 0-60 kbar. At room temperature, the dependence of the quantum-well photoluminescence peak on pressure is sub-linear. It is linear at liquid-nitrogen temperature. The pressure coefficient is approximately 10 percent less than that of the GaAs barrier. The pressure coefficient of the photoluminescence peak corresponding to the second sub-band of the conduction band is slightly larger than that of the first sub-band. This is opposite to the results obtained with $GaAs/Al_xGa_{1-x}As$ quantum wells.

I. Introduction

The study of $In_xGa_{1-x}As/GaAs$ strained quantum well superlattices has aroused much interest in recent years.[1] Since lattice matching is not required between the potential well and potential barrier materials in a strained quantum well superlattice, there are more choices in the design of quantum-well energy band structures. Thus, it brings bright prospects to the design and utilization of new materials and devices. The energy band of the $In_xGa_{1-x}As$ layer is distorted due to the two-dimensional strain caused by a mismatch in lattice constants.[2] Some new characteristics introduced from the splitting of the valance band also generate additional interest.

Photoluminescence under hydrostatic pressure is an effective technique for studying semiconductor band structure. It has been successfully used in studying GaAs/$Al_xGa_{1-x}As$ quantum-well structures.[3-6] However, we have not seen any articles on $In_xGa_{1-x}As$/GaAs. This paper is the first report on the photoluminescence behavior of $In_xGa_{1-x}As$/GaAs strained quantum-well structures under static pressure. Pressure coefficients of photoluminescence peaks, which are related to the quantum well, were obtained. A decrease in luminescence efficiency due to Γ-X crossing was observed. The results are briefly discussed.

II. Experimental Method

All specimens are $In_xGa_{1-x}As$/GaAs SSQW grown by MBE [molecular beam epitaxy]. The substrate is [100] semi-insulating GaAs. The first layer grown was a 0.5-μm-thick buffer layer. Then, we put on a single layer of $In_xGa_{1-x}As$ quantum wells. Finally, a 500-Å-thick GaAs layer was grown to cover it. All epitaxial layers were not doped. The growth temperature was 530-550°C. Table 1 shows the X values and well widths of the specimens. Photoluminescence measurements made at 10 K confirmed their excellent optical characteristics.

Table 1. Pressure coefficients by least square fitting

Fitting Equation		$E = E_0 + \alpha P + \beta P^2$ (300K)		$E = E_c + \alpha P$ (300K)	$E = E_0 + \alpha P$ (77K)	
Specimen	Peak	α (meV/kbar)	β ($\times 10^{-2}$meV/kbar^2)	α (meV/kbar)	α (meV/kbar)	α_x (meV/kbar)
#1180 $x = 0.18$ $L_z = 130$ Å	E_{1h}	11.8±0.2	−4.6±0.3	8.7±0.1	8.1±0.1	−1.43
	E_{2h}	11.3±0.3	−3.5±0.6	9.5±0.1		−1.60
	E_s	12.6±0.4	−4.6±0.8	10.4±0.1	9.4±0.2	−1.49
	$E_{2h} - E_{1h}$			0.16±0.03		
	$E_s - E_{1h}$			0.85±0.05	0.80±0.05	
#1182 $x = 0.165$ $L_z = 180$ Å	E_{1h}	12.5±0.3	−5.6±0.4	8.9±0.1	8.4±0.1	−1.11
	E_{2h}	11.7±0.6	−3.9±1.0	9.6±0.1		−1.84
	E_s	12.4±0.3	−4.0±0.5	10.4±0.1	9.1±0.2	−1.43
	$E_{2h} - E_{1h}$			0.14±0.1		
	$E_s - E_{1h}$			0.80±0.1	0.80±0.07	
Bulk GaAs		12.5±0.5[8] 12.6[9]	−3.7±0.5[8] −3.77[9]		10.7[6]	−1.34[6]

The pressure device uses a head-to-head diamond structure. Details of the experimental method and optical system are given in reference [7]. The 4880-Å light from an Ar^+ laser was used for excitation at an intensity of 10^3-10^4 W/cm^{-2}. The photomultiplier was an RCA C31034A with a GaAs cathode.

III. Results and Discussion

Figures 1 and 2 show the photoluminescence spectra of sample #1180 (X=0.18, L_z=130 Å) under various pressures at room and liquid-nitrogen temperatures, respectively. The spectra for sample #1182 is basically the same. Because of the limitation of the spectral response of the photomultiplier, photoluminescence from $In_xGa_{1-x}As$ quantum wells could be measured only above a certain pressure. Three photoluminescence peaks, E_{1h}, E_{2h} and E_s, correspond to the photoluminescence between the n=1 and n=2 sub-bands of the conduction band and the n=1 sub-band of the heavy-hole band, and the photoluminescence of the GaAs barrier, respectively. At a liquid-nitrogen temperature, only E_{1h} was observed and E_s was very weak. These peaks shifted toward higher energy with increasing pressure. Their intensities weakened and disappeared after exceeding a certain pressure. Under our experimental conditions, we did not observe any peaks related to indirect transition.

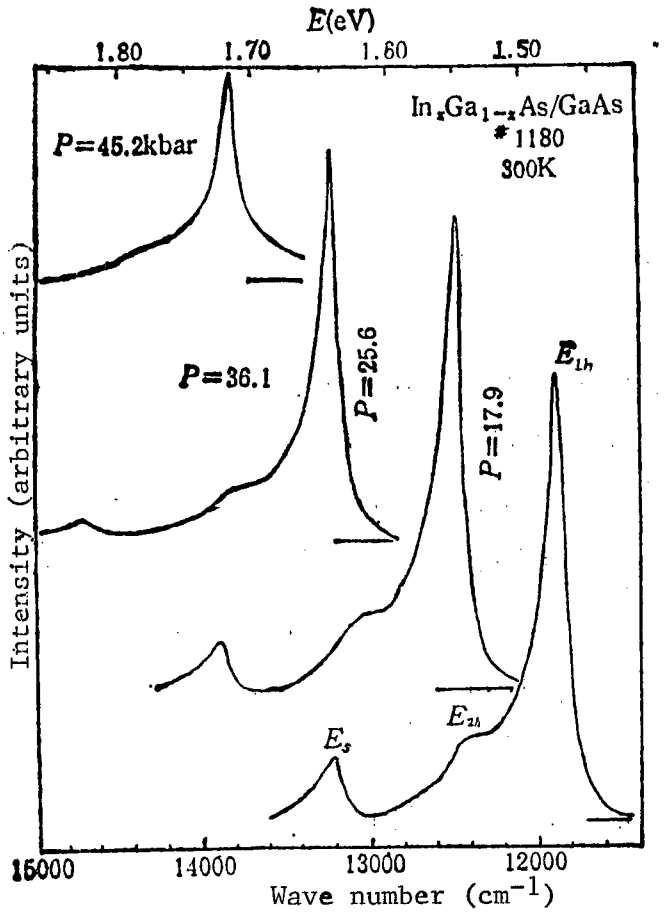

Figure 1. Photoluminescence spectra under different pressures at room temperature

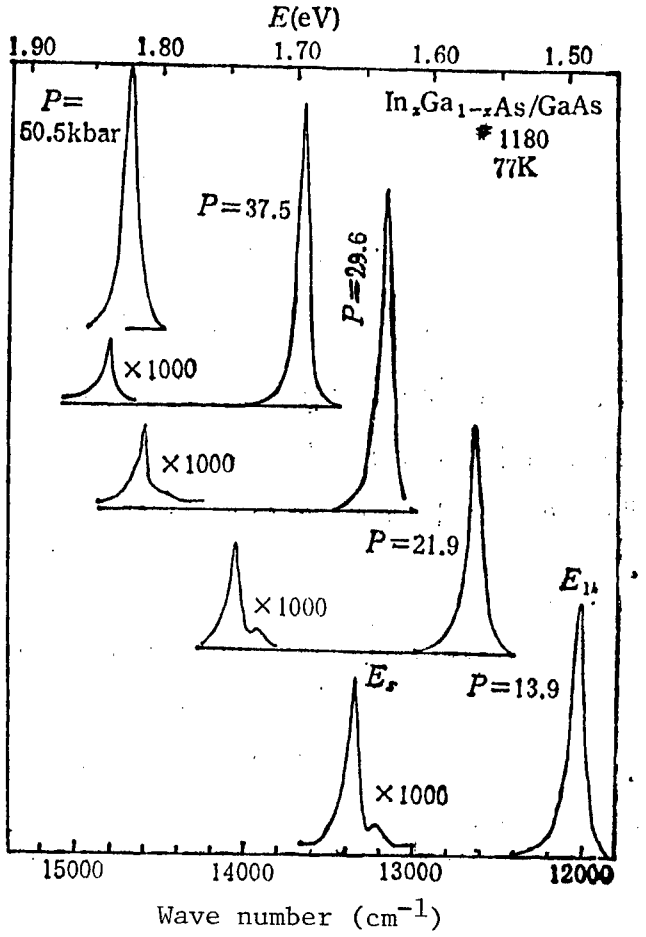

Figure 2. Photoluminescence spectra under different pressures at liquid-nitrogen temperature

Figure 3(a) shows the dependence of peak energy on pressure at room temperature. It is obvious that they are sub-linear. The solid lines are fitted based on $E = E_0 + \alpha P = \beta P^2$. The pressure coefficients obtained are shown in Table 1. The table also includes results obtained using a linear fit $E = E_0 + \alpha P$. The sub-linear pressure behavior of GaAs at room temperature has been observed by M. Leroux et al.[8] and B. Welber et al.[9] in photoluminescence and photoabsorption experiments, respectively. The pressure coefficients derived by them are also reported in Table 1. Our GaAs barrier value also agrees with theirs, indicating the absence of strain in the GaAs barrier layer. U. Venkateswaran et al.[10] found that the pressure behavior of E_{1h} in $GaAs/Al_xGa_{1-x}As$ multiple quantum well structures was linear at 300 K; however, they did not discuss the reason. We found that the pressure characteristics of E_{1h} and E_{2h} are sub-linear at room temperature as with GaAs. Whether this reflects any strain effect is yet to be investigated.

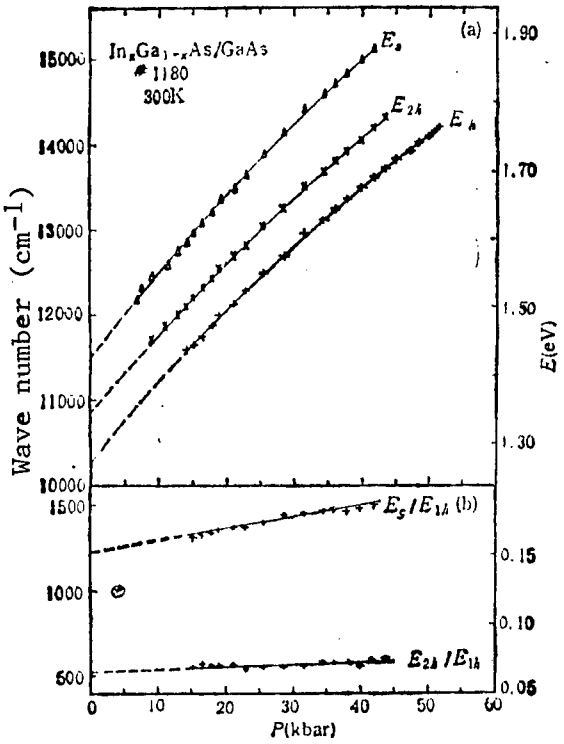

Figure 3. (a) peak energy vs. pressure at room temperature
(b) E_s-E_{1h} and E_{2h}-E_{1h} vs. pressure at room temperature

In order to clearly distinguish the difference of the pressure coefficients for these three peaks, Figure 3(b) illustrates the dependence of E_{2h}-E_{1h} and E_s-E_{1h} upon pressure. The solid lines are first-order fits and the fitting parameters are shown in Table 1. The pressure coefficient of the photoluminescence peak from the $In_xGa_{1-x}As$ quantum well is approximately 10 percent less than that of the GaAs barrier. Because the pressure coefficient of InAs is smaller than that of GaAs,[10] this is primarily due to the difference in their pressure coefficients. Since the pressure coefficient of bulk $In_xGa_{1-x}As$ is not available, it is very difficult to estimate the effect of quantization and strain on the pressure behavior. We can also see from the figure that E_{2h}-E_{1h} shows a slight increase with pressure, indicating that the pressure coefficient of the E_{2h} peak is slightly larger than (by approximately 1.5 percent) that of the E_{1h} peak. This is opposite to the situation with the $GaAs/Al_xGa_{1-x}As$ quantum well; this point will be investigated later. In the $GaAs/Al_xGa_{1-x}As$ quantum well, the pressure coefficient of the E_{2h} peak is smaller than that of the E_{1h} peak. This decrease and the fact that the pressure coefficient of E_{1h} decreases with decreasing well width have been interpreted as arising from the different pressure coefficients at various energy points in the valley corresponding to these sub-bands.[3] In narrow wells (< 50 Å), some effect is due to the fact that a part of the wave function expands to the barrier region where the pressure coefficient is small.[4] The results we obtained, however, do not agree with the model where higher energy points in the Γ valley have smaller pressure coefficients. Furthermore, the well

is relatively wide. Although the pressure coefficient of the barrier material is larger than that of the potential well, the wave function nevertheless does not propagate much into the barrier; it does not seem to cause the above result. More experiments and theoretical computation are required.

Figure 4 shows how various peak intensities vary with pressure at room temperature. The intensities of E_{2h} and E_s relative to that of E_{1h} are also shown in the insert in the same figure. We can see that the photoluminescence intensity drops rapidly when the pressure exceeds a certain value. This reflects the decrease in photoluminescence efficiency when electrons go through the transition from the Γ valley to the X valley. Based on the relative intensities of E_{2h} and E_s to that of E_{1h}, Γ-X crossing in the GaAs barrier occurs earlier than that in $In_xGa_{1-x}As$. This is consistent with the fact that the energy difference between the Γ and X valleys is larger with InAs. Since the n=2 sub-band is on top of the n=1 sub-band, the effect of the X valley also takes place earlier. Hence, E_{2h}/E_{1h} first drops and then bounces back.

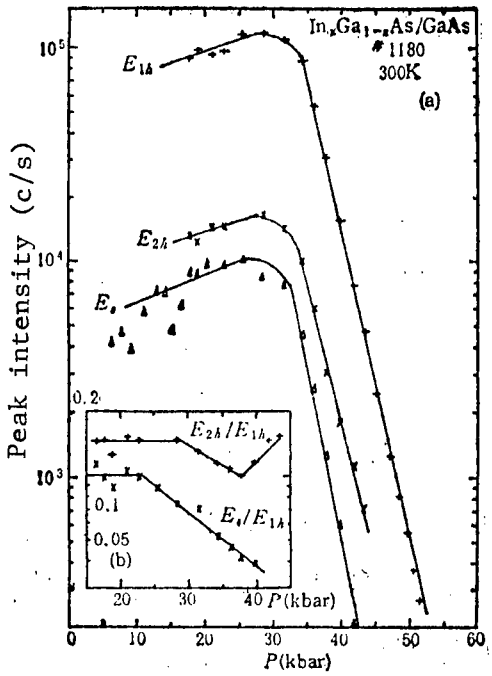

Figure 4. (a) peak intensity vs. pressure at room temperature
(b) relative intensity E_s/E_{1h} and E_{2h}/E_{1h} vs. pressure at room temperature

The variation in photoluminescence intensity due to electron distribution between the Γ and X valleys can be expressed as:[11]

$$I = I_0\{1 + A\exp[(\alpha_\Gamma - \alpha_x)(P - P_0)/KT]\}^{-1}$$

where I_0 and A are constants, and α_Γ and α_X are the pressure coefficients for the Γ and X valleys, respectively. Based on the Γ-valley pressure coefficient and photoluminescence intensity measured, it is possible to derive the X-valley pressure coefficient. The results are also shown in Table 1. The result is consistent with the fact that the X valley shifts toward lower energy with increasing pressure. However, because we are limited by the accuracy of photoluminescence intensity measurement, it is relatively hard to compare the difference in pressure coefficients between the GaAs barrier and $In_xGa_{1-x}As$.

Figure 5 shows how each peak energy varies with pressure at a liquid-nitrogen temperature. Unlike at room temperature, they are linear at the liquid-nitrogen temperature. Pressure coefficients obtained by least square fitting are also shown in Table 1.

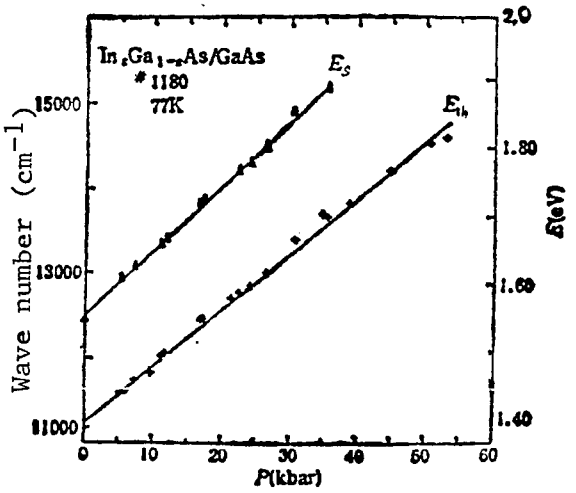

Figure 5. Peak energy vs. pressure at liquid-nitrogen temperature

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Self-Consistent Calculation of Electron Concentrations in GaAs/AlGaAs Quantum Well Structures

40080216a Beijing BANDAOTI XUEBAO [CHINESE JOURNAL OF SEMICONDUCTORS] in Chinese Vol 10 No 5, May 89 pp 350-355

[Article by Yang Yuefei [2799 1878 7236], Zhu Weiwen [2612 5588 7186] and Wang Weiyuan [3769 3262 3293] of the Shanghai Institute of Metallurgy, Chinese Academy of Sciences, manuscript received on 6 Feb 88, funded by the Chinese Academy of Sciences: "Self-Consistent Calculation of Electron Concentration in GaAs/AlGaAs Quantum Well"]

[Excerpts] Abstract

The potential distribution, sub-band levels, 2DEG (2-dimensional electron gas) concentration distribution and 2DEG surface concentration n_s, as well as their relationship with parameters such as quantum-well width and undoped AlGaAs layer thickness, are self-consistently calculated for a modulation-doped AlGaAs/GaAs/AlGaAs quantum well using a wave-function expansion method. It was found that the 2DEG n_s in the quantum well is approximately two times [i.e., 200 percent] higher than the n_s at a single heterojunction. When the quantum-well width is between 200 and 300 A, n_s has a maximum. When the quantum well is too wide, the 2DEG is concentrated near the heterojunction interface to become a double heterojunction.

Key words: Modulation-doped quantum well, GaAs/AlGaAs heterojunction, 2DEG concentration.

I. Introduction

The high electron mobility transistor (HEMT) has been widely used in high-speed electronic devices in recent years. However, since the conventional HEMT is fabricated with single-heterojunction GaAs/AlGaAs, further improvement of its performance is limited by the 2DEG n_s, electron saturation speed v_s, and the dependence of mobility $\mu(E)$ upon the electric field.[1,2] v_s and $\mu(E)$ are determined by the characteristics of the material. Hence, raising n_s is an important way to improve the performance of the HEMT. With regard to raising the 2DEG n_s, preliminary experimental results were obtained in a double-heterojunction GaAs/AlGaAs quantum well HEMT[2,4]. Moreover, this type of HEMT power device has been built. It was found to have high n_s, high output

current density and large transconductance.[5] Although theoretical calculations for a quantum well HEMT have been reported, most have concentrated on the electron-wave distribution in the quantum well.[6] Or, n_s is fixed at a certain value in the calculation.[7] The relationship between n_s and the modulation parameters has not been reported. This paper employs a wave-function expansion technique to self-consistently calculate the potential distribution, sub-band levels, 2DEG concentration distribution and n_s in the modulation-doped AlGaAs/GaAs/AlGaAs quantum well and their relationship with material parameters such as quantum-well width and undoped AlGaAs thickness. [Passage omitted]

III. Results and Discussion

Figure 2 shows how n(x) [2DEG concentration distribution function] and V(x) [electron potential-energy function] vary with the quantum-well width [2a] at a given N_d [donor dopant concentration in the n-AlGaAs] (= $1x10^{18}$ cm^{-3}) and W_{sp}[undoped AlGaAs thickness] (= 50 Å). When the well width is 100 Å, 2DEG is concentrated in the middle of the quantum well. When the well width is 200 Å, 2DEG is flat. As the width increases further, 2DEG is primarily concentrated near the heterojunction interface; it thus becomes a double heterojunction (see Figure 2(d)). As the well width increases, occupancy of electrons in the sub-bands also extends from ground state to the first and second excited states. In addition, the bulge at the bottom of the well also gets larger with increasing width.

Figure 3 shows the dependence of 2DEG n_s upon well width. n_s is at maximum when the quantum-well width is in the range of 200-300 Å. n_s decreases when the width is either too narrow or too wide. Furthermore, when the quantum well is too wide (e.g., 500 Å), 2DEG is concentrated near the interface of the two heterojunctions to form a double conductive channel. Thus, the normal gate-control characteristics of the HEMT will be affected. For instance, the curve of transconductance versus gate bias of a multi-channel HEMT has low valleys.[4] Hence, choosing a proper quantum well width to maximize n_s benefits performance of the HEMT.

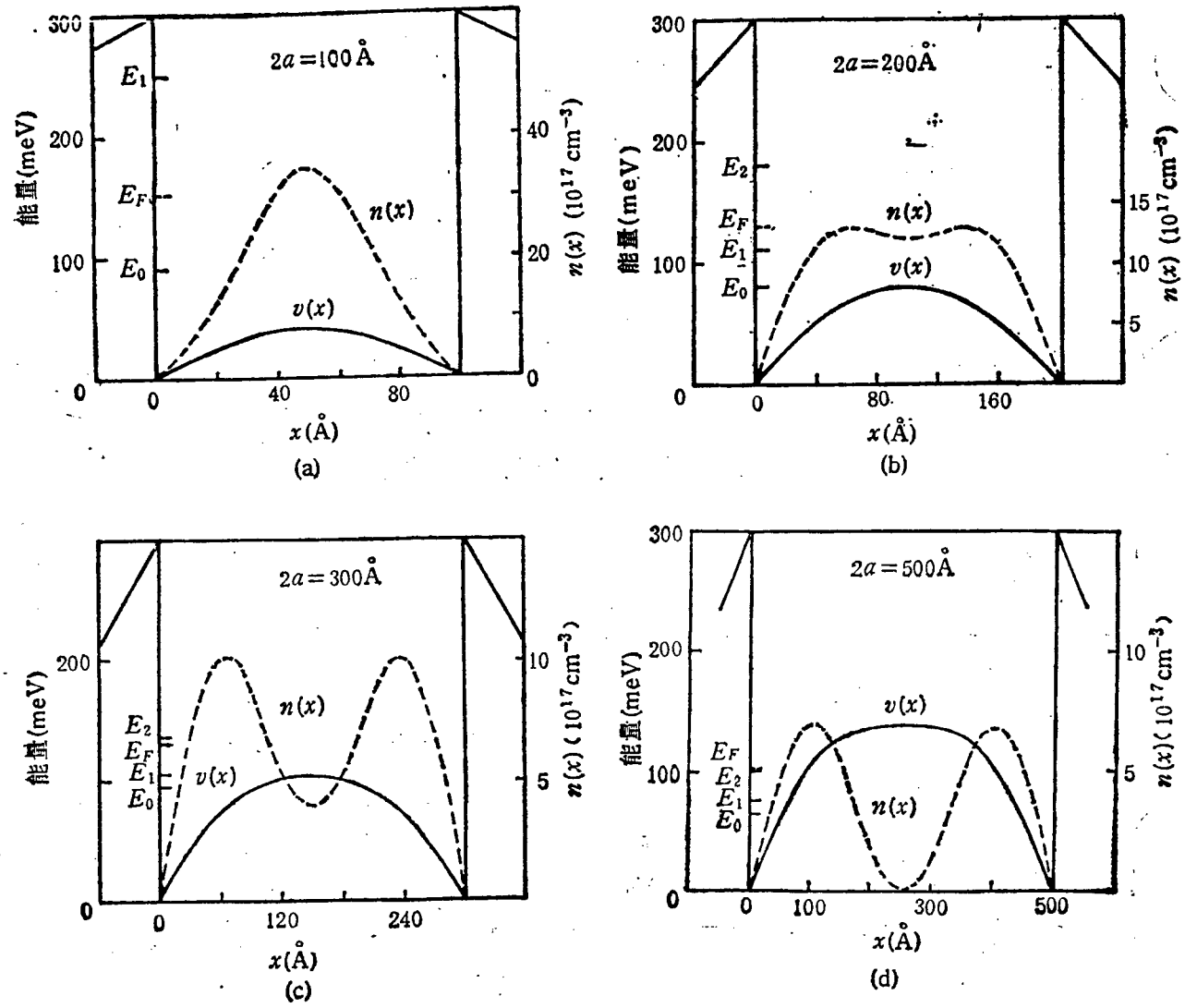

Figure 2. n(x) and V(x) curves in quantum well.

(N_s = 1x10^{18} cm^{-3}, W_{sp} = 50 Å)

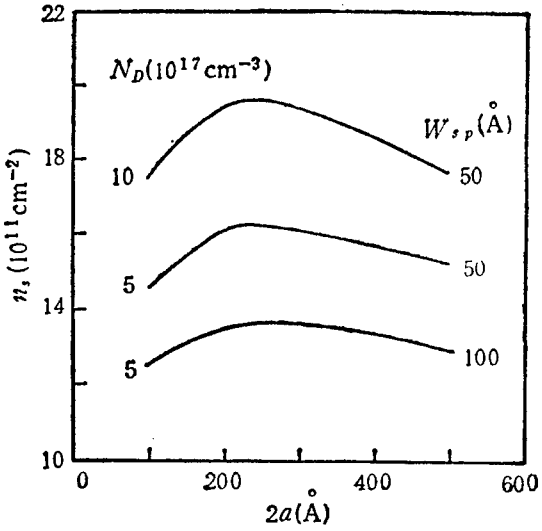

Figure 3. n_s versus quantum-well width

Figure shows the dependence of n_s upon undoped AlGaAs thickness. In addition, the result of a single heterojunction is also given. A comparison shows that the n_s in the well is approximately 200 percent higher than the n_s in a single heterojunction.

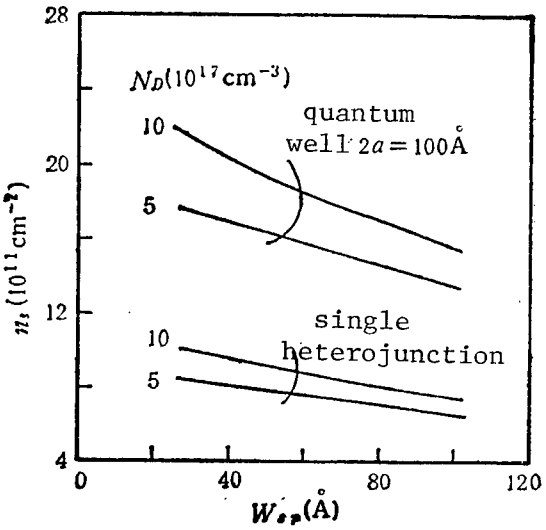

Figure 4. n_s versus undoped AlGaAs thickness

Table 2 is a comparison of experimental n_s values reported in the literature to the calculated results in this work. The calculated results are in good agreement with the results reported in reference [4] and they deviate from the results given in reference [3] by a certain amount. The primary reason is due to the presence of an error in the experimental value for N_s. Furthermore, the experimental value for E_s [activation energy of donor impurities in the AlGaAs] is not defined and it is dependent upon the growth conditions, degree of impurity compensation and dopant concentration.[12,13] Therefore it is not possible to obtain the correct δ [difference between conduction band in the AlGaAs and the Fermi energy level]. Moreover, this work only considers the ideal situation. In a real quantum well material, GaAs contains a certain concentration of impurities; there are surface states at the GaAs/AlGaAs interface and there is a transition zone at the heterojunction interface. These are factors which lower n_s. Therefore, it is reasonable for the experimental values to be lower than the theoretical values.

Table 2. Experimental and Theoretical Results of ns (77 K)

2a(Å)	W_{sp}(Å)	N_s (10^{17} cm^{-3})	n_s(10^{11} cm^{-2})exp.	ref.	n_s(10^{11} cm^{-2})calc.
300	50	10	18	[4]	19.3
300	100	10	12.7	[3]	15.8

The situation where modulation-doping parameters are not taken into account and n_s is fixed has been numerically calculated.[14] Similarly, when we do not consider equation (6) and keep n_s fixed, a comparison of the results with those reported in reference [14] tells us that the difference in V(x) is not significant. The $|\psi_0(x)|^2$ and $|\psi_1(x)|^a$ obtained in this work are slightly shifted toward the center of the quantum well. The major reason is that we neglected the penetration of the wave function across the AlGaAs. However, the wave function distribution is very similar. Therefore, the results satisfactorily reflect the 2DEG concentration distribution, potential distribution and sub-band splitting of the modulation-doped quantum well.

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Experimental Research on Si/a-Si:H Heterojunction Microwave Bipolar Transistor

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[Article by Wang Yinsheng [3769 0936 3932], Sheng Wenwei [4141 2429 0251], Wang Jianyuan [3076 1696 0337], Zhang Xiaoming [1728 2556 2494], Xiong Chengkun [3574 2110 1024] of the Nanjing Institute of Electronic Devices, and Zhu Enjun [2612 1869 0971] of the Institute of Microelectronics, Beijing University, manuscript received on 9 Dec 88: "Experimental Research on Si/a-Si:H Heterojunction Microwave Bipolar Transistor"]

[Text] Abstract

The fabrication and characteristics of a silicon microwave heterojunction bipolar transistor (HBT) with a heavily doped amorphous hydrogenated silicon (n^+ a-Si:H) emitter are reported for the first time. The base sheet resistance of the device is 2 k$\Omega/\square$[kilohms per square], base width is 0.1 μm, and the maximum common emitter current gain is 21 (V_{ce} = 6 V, I_c = 15 mA). The emitter Gummel number G_E has reached 1.4×10^{14} Scm^{-4}. The S parameter measured indicates that the current-gain cutoff frequency f_t = 5.5 GHz and the maximum oscillation frequency f_{max} = 7.5 GHz. To date, in the literature on the Si/a-Si HBT, this is the first amorphous silicon-emitter heterojunction bipolar transistor that can operate in the microwave band.

Key words: amorphous hydrogenated silicon, heterojunction, microwave bipolar transistor.

Heterojunction bipolar transistors (HBTs) have attracted a great deal of interest among researchers because they have a bright prospect for use in the high-frequency, high-speed domain. In addition, significant success has been achieved with HBTs using III-V semiconductor materials. Because silicon is cheap and flat silicon fabrication technique is mature, the silicon HBT has received wide attention. Recently, a Si/a-Si HBT has been reported.[1-4] These research reports primarily focused on the a-Si/c-Si heterojunction interface and the dc characteristics of the HBT. The high

forward injection at the heterojunction is used to obtain high current gain and low base resistance. Furthermore, it is projected this device will have better high-frequency characteristics. However, the high-frequency characteristics of the a-Si HBT have not been reported to date. This paper reports the fabrication and characteristics of a microwave Si/a-Si:H HBT using a heavily doped a-Si:H emitter and a base prepared by the conventional boron diffusion technique.

a-Si:H and a-SiC are the two primary amorphous silicon materials used as the emitter of a silicon HBT. This work used a-Si:H as the forbidden-band emitter material. It is believed, based on existing experimental and theoretical results, that hydrogen atoms in a-Si:H can compensate for the dangling bonds in amorphous silicon due to the presence of defects. Consequently, the density of the gap state is lowered to facilitate controllable doping. The preparation of a-Si:H in this experiment was done in an external-capacitance coupled glow discharge system (model PECVD 1002, made in China). The advantage of the system is that it minimizes radiation damage to the silicon wafer from the high-frequency electric field. X-ray diffraction analysis of the a-Si:H samples prepared in this experiment showed no crystal diffraction peaks in the range of 10-40°. Raman spectra of the specimens showed the presence of a wide band near 480 cm^{-1}, which is an envelope characteristic of amorphous silicon. Moreover, peaks corresponding to single and poly-crystalline silicon in the vicinity of 520 cm^{-1} were not observed. Therefore, it was confirmed that the specimen is amorphous, instead of polycrystalline or microcrystalline silicon. The SiH_4 and PH_3 used in the experiment were diluted with high-purity H_2. In the deposition process, the H_2-SiH_4-PH_3 flow rate must be carefully controlled in order to grow a thin layer of amorphous silicon. The thickness of the thin layer is approximately 3000 Å and the average resistance was controlled at about 0.5Ωcm.

The band gap of amorphous silicon varies with the technique and condition. The optical band gap of the a-Si:H obtained in this work is between 1.65 and 1.85 eV. It is 1.12 eV for single-crystal silicon. The emitter material n^+ a-Si:H was deposited on a base of P-type single silicon at low temperature (T = 270°C) to form an emitting step heterojunction. Based on the H. Kroemer theory, the injection of holes from base to emitter must overcome the discontinuous valence band potential barrier ΔE_v. Thus, hole injection is greatly reduced. Therefore, high current gain can still be achieved even with a heavily doped base and lightly doped emitter. A simple derivation reveals that the emitter injection-limited current gain β_r can be expressed as:

$$\beta_r \quad \frac{L_E R_{\square B} \mu_{PB} \mu_{nB} N_{CB} N_{vB}}{W_E R_{\square E} \mu_{PE} \mu_{nE} N_{cE} N_{vE}} \exp(\Delta E_v / kt)$$

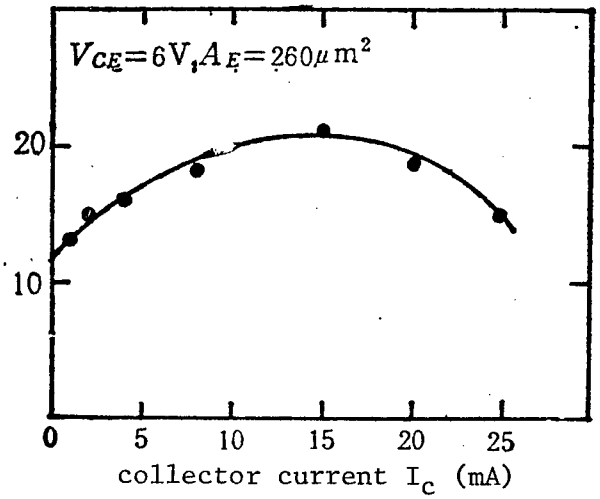
$$(L_B \gg W_B,\ W_E \gg L_E)$$

where the above are commonly used symbols. L_E and L_B are emitter and base minority carrier diffusion lengths. W_E is the emitter layer thickness and W_B is the base width. In addition, we have the following equations:

$\Delta E_v = \Delta E_c$, $\Delta E_g = E_{g2} - E_{g1}$, and $\Delta E_c = \chi_1 - \chi_2$ (subscript 1 and 2 represent single-crystal and amorphous silicon, respectively).

Based on the properties of silicon and amorphous silicon, if ΔE_g = (1.65-1.10) eV = 0.55 eV and ΔE_c = (4.05-3.93) eV = 0.12 eV, then ΔE_v = 0.43 eV. At room temperature, $\Delta E_v/KT \simeq 17$. The value of β_r is primarily determined by the term exp ($\Delta E_v/KT$) which is large. This indicates that very high current gain can be obtained without considering the emitter-to-base doping ratio. In a homojunction, $\Delta E_v = 0$ and $\beta_r \sim R_{\square B}/R_{\square E}$. In order to ensure the current gain, base sheet resistance cannot be too low. Limiting the base dopant concentration would affect the microwave gain and high-current characteristics of the device. In other words, a Si/a-Si:H HBT allows the use of a higher base doping concentration to improve its microwave characteristics. The base surface concentration of the experimental device has reached 1 x 10^{19} cm^{-3}. The maximum current gain is 21 (V_{CE} = 6V, I_c - 15 mA). The corresponding current density is 5.8 x 10^3 Acm^{-2} (A_E = 260 μm^2). Based on the characteristics of the device, the Gummel number G_E of the emitter was calculated to be 1.4 x 10^{14} Scm^{-4}. The G_E of a homojunction bipolar transistor is usually less than 5 x 10^{13} Scm^{-4}. This indicates that at the same base Gummel number, the current gain of a Si/a-Si:H HBT is significantly better than that of a silicon homojunction device.

Figure 1 shows the common emitter current gain h_{FE} verses collector current I_c curve of a Si/a-Si:H HBT. The common emitter output characteristics are shown in photograph in Figure 2 [photograph not reproduced].



current gain h_{FE}

Figure 1. h_{FE} vs. I_c curve for a Si/a-Si:H HBT

The offset voltage between the collector and emitter of the device was measured to be around 60 mV. When V_{CE} is below this value, no current flows. This is because the emitter-base heterojunction has a higher bias than the base-collector homojunction.

Measurements of the diode n value of the emitter junction revealed that the ideal diode n value was approximately 1.01 at between 30 μA and 1 mA. At higher currents (5 - 20 mA), the corrected n value is in the range of 1.5 - 2.0. At low currents ($<$30 μA), n apparently deviated from its ideal value, reflecting larger contribution of carrier recombination at the heterojunction. The device must be annealed at a low temperature (e.g., 280°C, 15 minutes, in nitrogen or nitrogen-hydrogen mixture) to allow the hydrogen atoms in the a-Si:H film to fill up the defect energy levels and broken bonds at the heterojunction; this lowers the surface state density at the interface to reduce the recombination current. The current gain was increased by 100-200 percent after annealing. Low current gain was improved even more.

The microwave characteristics of the device were measured and calculated by using an HP-8510 automatic network analyzer. The wafer was mounted on a standard microstrip tube shell and connected to a test fixture in the common emitter mode to measure the S parameter between 404 MHz and 8 GHz. The forward current gain h_{21} was then calculated based on the S parameter. Figure 3 shows the dependence of $|h_{21}|$ upon frequency f. From the figure we know that the cutoff frequency for current gain is f_t = 5.5 GHz. The one-way power gain of the device G_u could also be calculated from the S parameter and the results are shown in Figure 3. In one-way power gain, the maximum oscillation frequency f_{max} = 7.5 GHz.

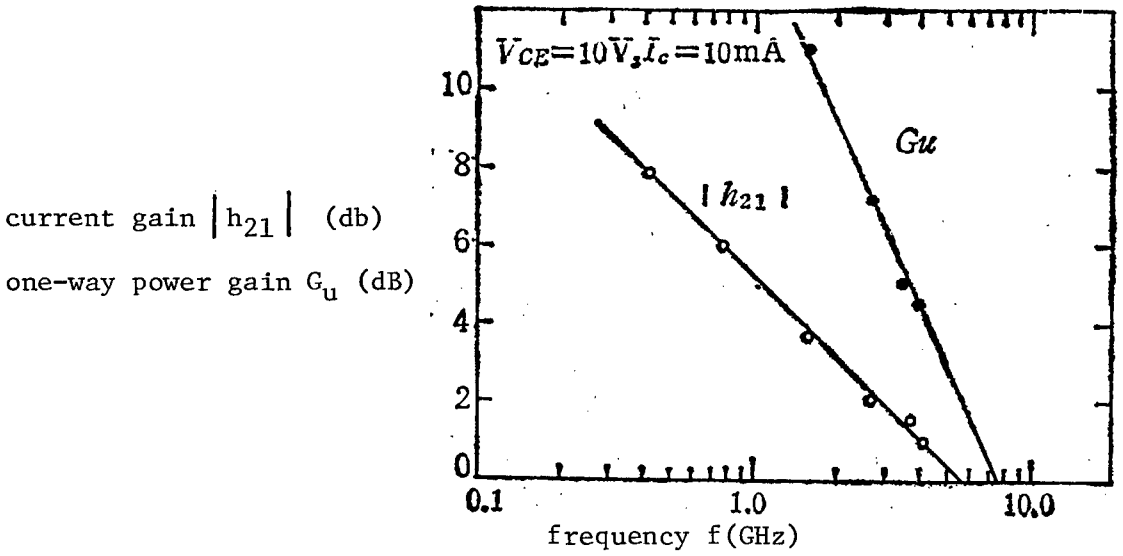


Figure 3. Dependence of forward current gain h_{21} and one-way power gain G_u on frequency f

f_t and f_{max} are two important frequency parameters for a microwave bipolar transistor. f_t is directly related to the vertical structure of the device. The product $V_{cE\ max} \times f_t$ is greater than 1.1×10^{11} V/s ($V_{CE\ max}$ = 21 V) for the experimental device. f_{max} is closely correlated to the transverse dimensions of the device. The transverse dimensions of the actual device are relatively large. The width of the emitter is 5.2 μm and the total emitter area A_E and total base area A_B are 260 μm[a] and 2460 μm[a], respectively. The emitter perimeter-to-base area ratio is E_p/A_B = 1.23 $mil.^{-1}$ This is far less than that of a conventional microwave transistor (i.e., 6 - 11 mil^{-1}). It is not too difficult to raise f_{max} further by properly reducing its transverse dimensions. A self-consistent scheme is proposed to reduce the base series resistance and base-collector capacitance. It was calculated that the f_{max} of this new device could be as high as 25 GHz.

In summary, a Si/a-Si:H HBT operating in the microwave region was fabricated by using a heavily doped amorphous hydrogenated emitter prepared by plasma glow discharge deposition. Our study on its dc and microwave characteristics suggests that amorphous hydrogenated silicon is one of the most promising forbidden-band emitter materials. An amorphous silicon-emitter heterojunction transistor is expected to be a promising device operating in the C band.

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Design of Millimeter-Wave Integrated Mixer

40080113a Beijing TONGXIN XUEBAO [JOURNAL OF CHINA INSTITUTE OF COMMUNICATIONS] in Chinese Vol 9 No 6, Nov 88 pp 21-27

[Article by Wu Wanchun* [0702 8001 2504] and Lu Qitang** [4151 0796 1016] of Xidian University [formerly Northwest Institute of Telecommunications Engineering], manuscript received 10 May 86: "Design of Millimeter-Wave Integrated Mixer"; project supported by funding from Ministry of Electronics Industry]

[Excerpts] Abstract

This paper presents a balanced millimeter-wave integrated mixer structure as well as a theoretical analysis and numerical computation of every component. An example of the balanced millimeter-wave integrated mixer at the 8-mm band is given. Based on preliminary results, the minimum noise factor F_{DSB} is 5.0 dB (including IF noise factor of 1.5 dB).

I. Introduction

As millimeter-wave technology is being developed and applied, researchers are focusing more on millimeter-wave integrated mixers, terminal et al. used E surface printed circuits to develop a finline single terminal and a balanced mixer[1,2] in the K_a band. Later, a hybrid-circuit finline dual balanced mixer covering 10-40 GHz was

* Wu Wanchun: Professor of electromagnetic engineering of Xidian University, Vice Chairman of Microwave Communications Committee of the China Communications Society; graduated from Department of Electrical Engineering at Beijing University and presently engaged in teaching and research in CAA and CAD of microwave semiconductor circuits and millimeter-wave circuits.

** Lu Qitang: received Master's degree from Northwest Institute of Telecommunications Engineering in 1985, currently employed by Xidian University as a lecturer.

developed[3] based on the E surface circuit technology. Integrated finline balanced mixers have also been developed in China[4] and the results have been satisfactory.

This paper introduces a relatively simple balanced millimeter-wave integrated mixer. Furthermore, theoretical analysis and design computation are done for each circuit component. In addition, an experimental design has been done using Chinese-made devices and wafers. Satisfactory frequency-mixing behavior was obtained.

Figure 1 shows the balanced integrated mixer design. It consists of four [labeled] parts: Part (1) is the transition from rectangular waveguide to the finline, part (2) is the transition from waveguide to finline and then to the micro-stripline, part (3) is the shielded micro-stripline and part (4) is the diode socket and its resonance circuit. From the local oscillation (LO) end, it is an isolated suspended stripline. From the signal end, it is a bipolar finline. Thus, it forms a magic T circuit. Based on theory, balanced mixing is achieved by applying an out-of-phase local-oscillation signal and an in-phase RF signal to two diodes. In addition, the local oscillation of the micro-strip input cannot be transmitted in the finline and the RF signal input from the finline cannot be transmitted in the micro-strip. Therefore, local oscillation is naturally isolated from RF signal. Figure 1 (a) shows the coaxial output of intermediate frequency (IF) signals with the micro-strip through the low-pass filter. [Passage omitted]

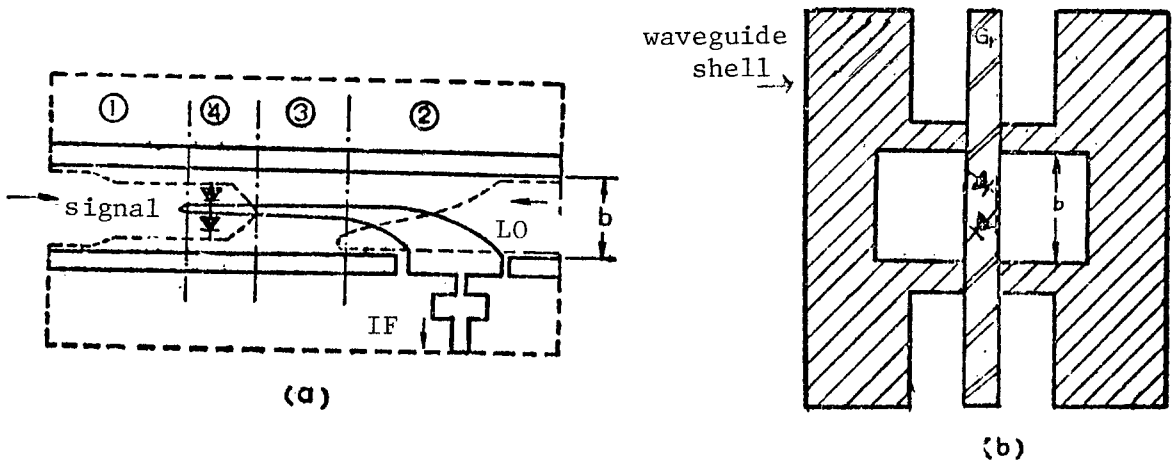

Figure 1. Mixer Circuitry

(a) integrated circuit, solid profile is the metal film on the front of the substrate and dotted profile is metal film on the back of the substrate.

(b) cross-sectional view of the rectangular waveguide under the integrated substrate.

V. Example of Mixer Design

Figure 8 shows an experimental circuit design of an 8-mm balanced mixer. The dielectric substrate is TFE coated with copper, 0.2 mm in thickness. The diode is a Model WH51 Schottky diode. The waveguide is BJ-320

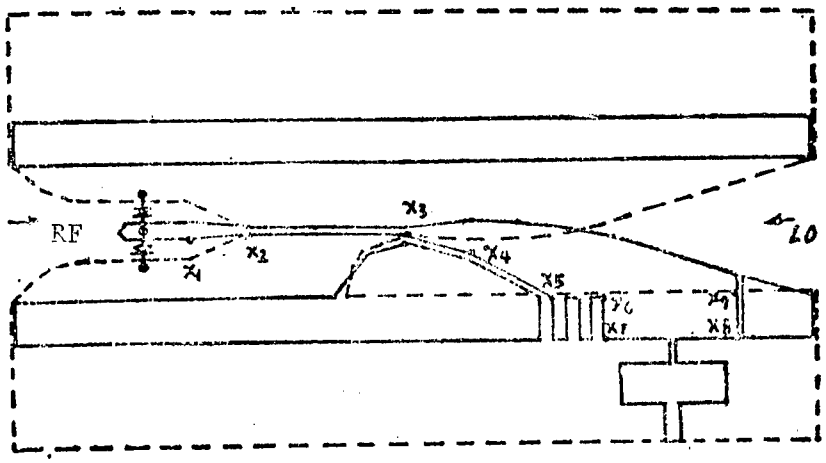

Figure 8. Actual Mixer Circuitry

front metal film inside solid lines, backside metal film inside dotted lines.

The design begins from the RF end. Under the excitation of the LO signal, the RF circuit of the mixer shown in Figure 9(a) is equivalent to that shown in Figure 9(b). R_e is the mean equivalent resistance of the diode and L_e is the equivalent inductance. The RF circuit should be matched according to:

$$Z_o = R_e$$

$$\omega L_e + Z_{o1} \tan (2\pi 1/\lambda_{g1}) \qquad (16)$$

where Z_{o1} is the impedance at the diode, λ_{g1} is the waveguide wavelength and 1 is the distance between the diode and the short circuit. Using either a frequency-transform matrix[10] or an approximation[11] technique, the equivalent resistance and inductance of the WH513 diode at 35 GHz are $R_e = 227\Omega$ and $\omega L_e = 580\ \Omega$, respectively, based on the parameters of the diode under excitation at local oscillation. Hence, the characteristic resistance of the diode with respect to the bipolar finline should be 227 Ω. In reality, it was chosen to be 246 Ω to take into consideration the size of the diode and to match with the LO circuit. Once Z_{o1} is known, the transversal dimension can be designed using the improved asymmetric impedance equation[6]. In addition, the transition from the single finline to waveguide was optimized using the method described in Section II. As a

result, when L = 6 mm and f is between 33 and 37 GHz, the voltage standing wave ratio $\rho_{max} < 1.008$. Furthermore, the distance 1 between the diode and the short-circuit point (x_2 in Figure 8) can be calculated based on equation (16).

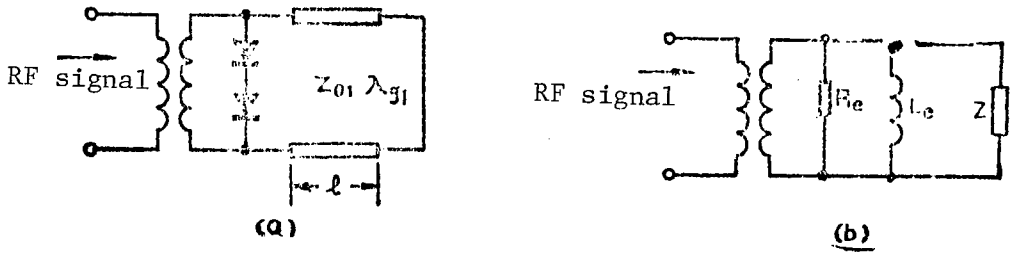

Figure 9. RF Equivalent Circuit of the Mixer

As for the LO circuit, the characteristic impedance of the isolated suspended stripline Z_{02} was calculated based on the dimension of the symmetric bipolar finline (x_1 in Figure 8) of the RF circuit: its value is 110 Ω. Then, the characteristic impedance Z_{03} (to the right of x_{02} in Figure 8) of the shielding micro-stripline was selected. It should be noted that Z_{03} could not be too high; otherwise, it would be difficult to match. Finally, a transition cone was added between Z_{02} and Z_{03} to ensure circuit match. In addition, it was necessary to design the transition from the micro-strip to the waveguide based on the method described in Section III. The length of the transition was chosen to be L = 15 mm. In the 32-38 GHz range, the voltage standing wave ratio $\rho_{max} < 1.07$.

The mixer circuit designed is shown in Figure 8. The dielectric substrate on the front and the metallized film pattern on the back are shown in the same figure. The shape of $x_3 \rightarrow x_4 \rightarrow x_5$ is determined to match the IF output circuit. The lower semi-circle was divided to prevent the formation of a resonance cavity and to facilitate the transition from the finline to the microstrip. The small slots to the right of the semi-circle are there to lower the capacitance in order to prevent IF short circuit. The small gaps x_8 and x_9 are also there to prevent IF short circuit.

The input impedance of the low-pass filter is a suspended-strip characteristic impedance with a width of $W = x_9 - x_5$. The output impedance is 50 Ω. In order to utilize the capacitance at $x_6 \rightarrow x_7 \rightarrow x_8 \rightarrow x_9 \rightarrow x_6$, we designed an n=3 variable capacitive input impedance low-pass filter.

Finally, the circuit substrate is in the middle of the E-plane of the waveguide. The external case of the waveguide is of conventional design.

After the mixer was developed, its noise index, isolation and voltage standing wave ration (VSWR) at the RF end were measured. Noise was measured by the IF attenuation method at 30 MHz. The results are shown in Figure 10. The noise curve includes IF amplification noise of 1.5 dB. The LO power was approximately 8 - 12 mW, which is close to its optimum.

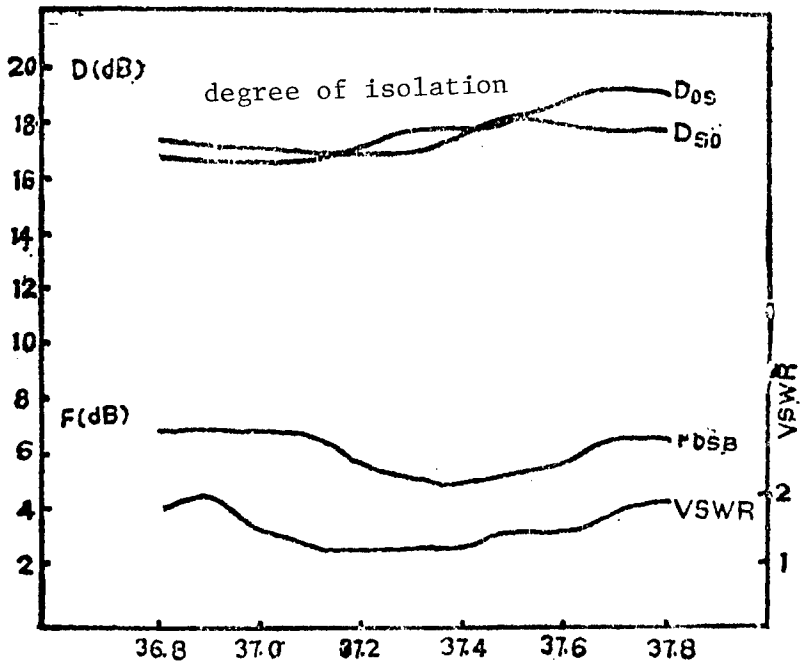

Figure 10. Performance Characteristics of the Mixer

The results indicate that the performance of the mixer designed is not ideal. The primary reason is that the components are not specifically designed for use at 8 mm, resulting in high frequency loss and large deviation in parasitic parameters. It is difficult to obtain a wide-band high-performance mixer. It only performed well at 35-38 GHz. In addition, because the tangent of the loss angle of the Chinese-made dielectric substrate is high, the noise index would be high. However, based on the performance of millimeter-wave receivers in the past year, its image is clearer than the so-called 4-dB-noise orthogonal field mixer on the market. Therefore, the noise index measured seemed to be believable. In terms of other characteristics, it is more superior to the orthogonal field mixer. If a better mixer tube and low-loss substrate are used, the performance of the mixer can be further improved.

VI. Conclusions

The structure of a balanced millimeter-wave integrated mixer has been analyzed in detail in this paper. The methods to calculate the transmission-line and transition-segment characteristics have been presented. An 8-mm-band mixer was developed. Its performance is satisfactory and consistent with the requirements for an 8-mm-band receiver. The mixer was successfully designed in one attempt which illustrates that the design approach is effective.

The authors wish to acknowledge the support they received from comrades at the 206th Institute of the Ministry of Ordnance Industry in the areas of design, processing and testing in this work.

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Non-Linear Analysis Method, Network Design for Microwave FET Broadband Power Amplifier

40080113b Beijing TONGXIN XUEBAO [JOURNAL OF CHINA INSTITUTE OF COMMUNICATIONS] in Chinese Vol 9 No 6, Nov 88 pp 28-32, 67

[Article by Zhao Jie* [6392 2212] and Li Zhengfan** [2621 1767 1581], manuscript received 25 May 87: "Non-Linear Analysis Method, Network Design for Microwave FET Broadband Power Amplifier"]

[Excerpts] Abstract

A non-linear equivalent circuit model for a GaAs FET [gallium arsenide field effect transistor] the help of dc current measurements, including drain-gate avalanche current. The convergence of the harmonic balance technique is discussed in detail. This technique is used to analyze a broadband microwave GaAs FET power amplifier, resulting in the non-linear analysis program NLINE.

Based on the non-linear model and the analysis, a 100 mW-output, 2-4 GHz broadband GaAs FET amplifier has been successfully designed and fabricated. The experimental data and theoretical prediction are in agreement.

* Zhao Jie is an assistant professor of electronic engineering at Shanghai Jiaotong University. He received his Master's degree from the electronic engineering department of Shanghai Jiaotong University in 1987 and is involved in teaching and research in microwave technology, electromagnetic field theory and microwave networks.

** Li Zhengfan is an associate professor of electronic engineering at Shanghai Jiaotong University. He graduated from the radio communications department of Ginghua University in 1958 and was a visiting scholar at Cornell University in 1981-83. He is involved in teaching and research in microwave technology, electromagnetic field theory and microwave network theory.

[See also Li Zhengfan, "Network Synthesis of Microwave FET Ultra-Broadband Amplifier," Shanghai SHANGHAI JIAOTONG DAXUE XUEBAO Vol 22 No 3, May 88 pp 46-52, translated in full in JPRS-CST-89-003, 31 Jan 89, pp 143-153]

I. Introduction

Microwave FET is a new device developed in recent years. A great deal of progress has been made in using it as a microwave low-noise amplifier (LNA) and a power amplifier in an active device. It is widely applied in communications, radar, remote sensing and instrumentation.

A broadband amplifier is required in many applications. With a microwave FET low-noise (small-signal) broadband amplifier, based on broadband matching network design theory, the design problem is essentially solved once the device's small-signal model or s parameter is determined. For a broadband power (or non-linear) amplifier, the problem concerning the non-linear FET model and the associated matching network design still exists. Under a specific non-linear distortion requirement, one has to maximize the power output and meet certain flatness requirements for gain and power output within a broadband range.

In this paper the non-linear microwave FET model is studied by current measurements and numerical fitting. The harmonic balance technique is used to analyze the broadband power amplifier and to present its convergence conditions. The optimum load of the matching network is obtained. It is used to guide us in the design of the broadband power amplifier.

A 2-4-GHz power amplifier was designed and fabricated based on the theory and program described above. Its performance characteristics met our expectations, consistent with the theoretical analysis.

II. Non-Linear Model for a GaAs FET

The internal structure of a GaAs FET is expressed by the equivalent circuit shown in Figure 1.

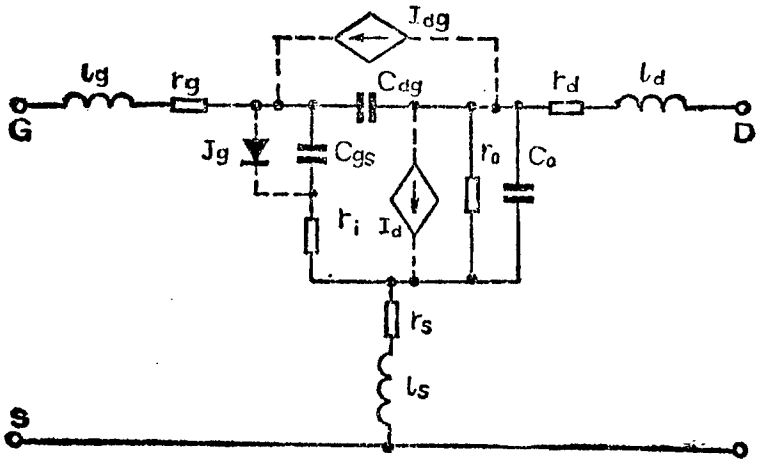

Figure 1. Non-Linear GaAs FET Model

I_g: represents the Schottky diode effect between gate and channel.

I_d: represents the control of gate on channel current source.

I_{dg}: represents the reverse breakdown effect between drain and gate.

r_g, r_d, r_s: represent ohmic contact resistance, r_i is the channel resistance, and l_g, l_d, l_s represent lead-wire inductance. C_o is the substrate capacitance. C_{gs} and C_{ds} are junction capacitances.

[Passage omitted]

III. Non-Linear GaAs FET Analysis Technique

Unlike a low-frequency amplifier, a microwave GaAs FET amplifier is fabricated on the transmission line. If we use a non-linear time-domain technique, problems such as the time-domain transmission model and slow convergence rate are unavoidable. The frequency-domain Volttra series method, however, is useful only when non-linearity is insignificant. Therefore, the harmonic balance technique was chosen to analyze the GaAs FET nonlinear circuit.

The harmonic balance technique is a method to treat the problem from time domain to frequency domain. As shown in Figure 2, the network is divided into a linear network and a non-linear network. The linear network is excited by a sinusoidal signal in the frequency domain and

the non-linear network is excited by a sinusoidal signal in the time domain. The harmonic component of the non-linear network is obtained by using a fast Fourier transform (FFT). The harmonics of the two networks are made consistent by iteration. By this time, the circuit parameters are also stable.

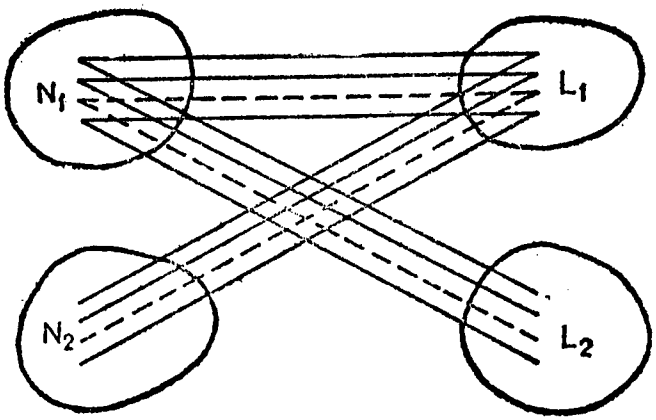

Figure 2

[Passage omitted]

Based on the harmonic balance technique and with the help of the FFT, the nonlinear analysis program NLINE was written to analyze the microwave GaAs FET and its associated network. It was written in FORTRAN 77 and run on an HP-1000 computer. The block diagram of the program is shown in Figure 4.

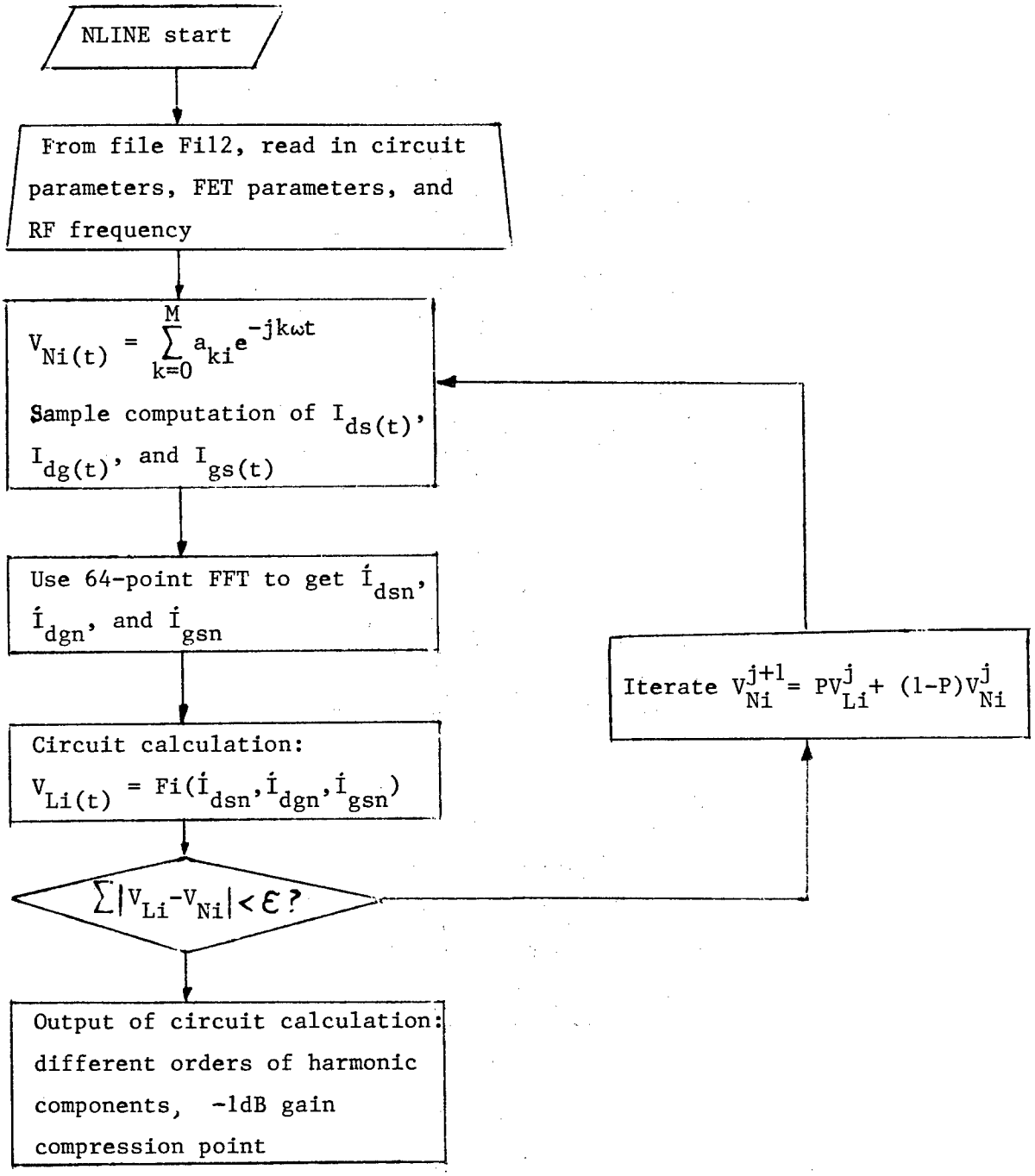
NLINE start
From file Fil2, read in circuit parameters, FET parameters, and RF frequency
$V_{Ni(t)} = \sum_{k=0}^{M} a_{ki} e^{-jk\omega t}$
Sample computation of $I_{ds(t)}$, $I_{dg(t)}$, and $I_{gs(t)}$
Use 64-point FFT to get $\dot{I}_{dsn}$, $\dot{I}_{dgn}$, and $\dot{I}_{gsn}$
Circuit calculation: $V_{Li(t)} = Fi(\dot{I}_{dsn}, \dot{I}_{dgn}, \dot{I}_{gsn})$
$\sum |V_{Li} - V_{Ni}| < \epsilon$?
Iterate $V_{Ni}^{j+1} = PV_{Li}^{j} + (1-P)V_{Ni}^{j}$
Output of circuit calculation: different orders of harmonic components, -1dB gain compression point

Figure 4

IV. Design of Matching Output Network

The matching output network should be designed to maximize the power output while keeping the broadband characteristics. Based on this requirement, we should obtain the optimum output load at every frequency point within the band and design a network which matches the load at different frequencies with 50 Ω. Although this technique is very precise, it is also very complicated. In this work the method is simplified.

The output portion of the GaAs FET model can be simplified as shown in Figure 4. Based on the quasi-static state concept under 10 GHz, the characteristics of I_{dg} do not vary with frequency. It is required that: $I_m(Z'_L) = 0$, $Re(Z'_L) = R'$. In addition C_o and l_d are absorbed by the matching output network.

With the help of the NLINE program, we analyzed the Chinese-made CX531 and its network. At -1dB compression gain, the load corresponding to maximum power output was found to be $Z'_L = 110$, as shown in Figure 5. A matching network could be designed accordingly using the same process as that for a small signal system.

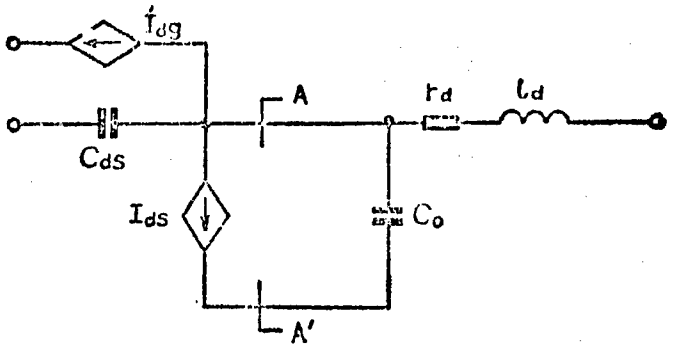

Figure 5

V. Experimental Results

Based on the method described above, through optimization, a 100-mW broadband power amplifier operating at 2-4 GHz was designed. Its FET is a CX531. Figures 6-8 are the circuit diagram, gain curve and power curve of the amplifier, respectively.

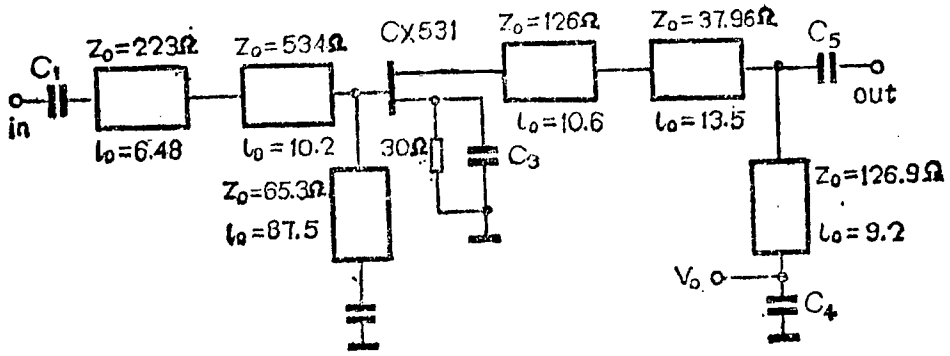

Figure 6

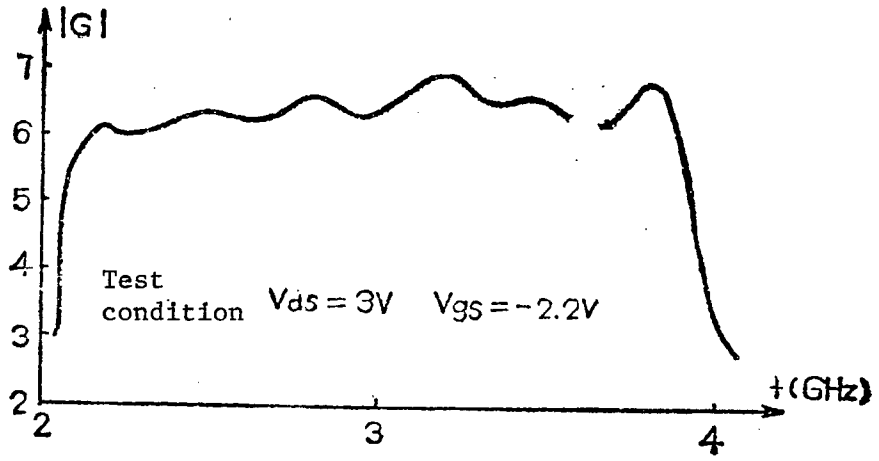

Figure 7

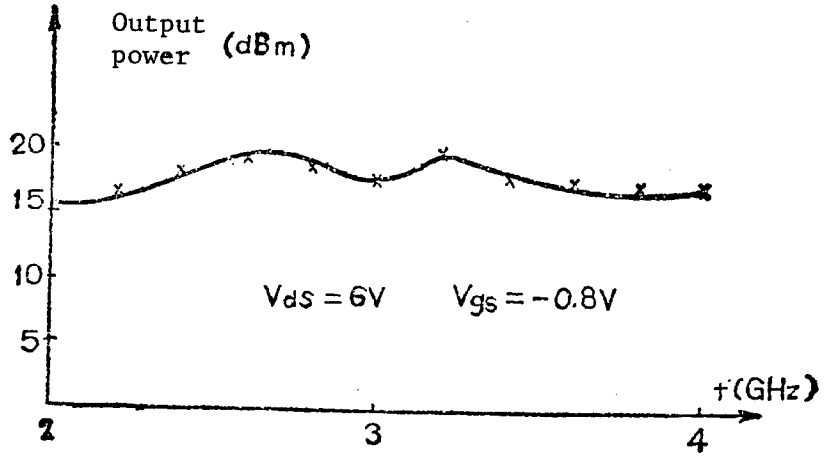

Figure 8

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Effects of Input VSWR of LNC on System Performance in Satellite Earth Station

40080113c Beijing TONGXIN XUEBAO [JOURNAL OF CHINA INSTITUTE OF COMMUNICATIONS] in Chinese Vol 9 No 6, Nov 88 pp 49-54

[Article by Chen Zhaowu* [7115 0340 2976] and Zhao Shihua** [6392 0577 5478], manuscript received on 3 Jul 86: "Effects of Input VSWR of LNC on System Performance of a Satellite Earth Station"]

[Excerpts] Abstract

The effects of the input voltage standing wave ration (VSWR) of an LNC (low noise converter) on the amplitude frequency response, carrier-to-noise ratio (C/N) and stability of the system are analyzed. These effects a reference for determining the VSWR of an LNC and for choosing an appropriate LNC.

I. Introduction

What should the input VSWR of the LNC of a satellite earth station be? There is no agreement on a specific value. If the input VSWR of the LNC needs to be less than 1.25, then a ferrite insulator must be added to the input end. However, in order to minimize the noise temperature of the LNC, the insertion loss must be as little as possible. In the C band, this insertion loss should be less than 0.13 dB. Its contribution to the noise temperature is approximately 10°K, which significantly raises the cost of the LNC. If an insulator is not used, the input VSWR is generally above 2. What is its effect on performance? What is a

* Chen Zhaowu: Associate Professor of Radio Communications at Qinghua University. He is involved in teaching and research in CAD of microwave circuits and hybrid integrated microwave circuit.

** Zhao Shihua: graduated from the Masters program in Radio Communications at Qinghua University in 1985; Lecturer of Radio Communications at Qinghua University. He is also involved in teaching and research in CAD of microwave circuits and hybrid integrated microwave circuits.

reasonable input VSWR of an LNC for satellite earth stations based on performance-to-cost ratio? These questions are discussed in this paper.

II. Effects on System Stability

All C-band low-noise FETs [field effect transistors], are intrinsically unstable. The low-noise amplifier may be inherently unstable if the design is improper. When the amplifier contact undergoes changes, self excitation may occur. If there is an insulator at the input end, then the stability of the system is not affected by the contact condition. In order to allow a low-noise amplifier without an insulator to function reliably and stably, advanced CAD techniques are required to look for a balance between stability and other parameters. The amplifier not only must meet certain stability requirements within its operating band, but also must remain somewhat stable outside the band. A simple method to verify the stability of an amplifier is to connect a sliding short circuit device or a variable load. The mode and phase of the reflective index of the load may be varied to simulate the antenna feed system of a satellite earth station. The amplifier is examined to determine whether it goes into self-excitation. If the amplifier is inherently unstable, but it is relatively stable in the neighborhood of the reflective index of the antenna-fed system, then it can still function reliably. For example, since the mode of the reflective index of the antenna-fed system generally does not exceed 0.1, an amplifier in which the mode of the reflective index at the head end does not exceed 0.5 would also be stable; this type of amplifier would never go into self-excitation. In general, a C-band satellite earth station can operate with absolute stability using a low-noise amplifier without an insulator as long as the design is carefully done. Table 1 shows the results of an analysis on the stability of an amplifier in its operating frequency band. From the centers and radii of the input and output stability circles shown in Table 1, the circle of instability is far from unity. Therefore, it is absolutely stable.

Table 1. Analysis of a Low-Noise Amplifier

Frequency (GHz)	Stable input circle			Stable output circle		
	Center		Radius	Center		Radius
	Mode	Phase angle		Mode	Phase angle	
3.70	3.00	−106	0.45	1.18	−52	0.07
3.80	5.34	− 88	1.35	1.65	− 25	0.09
3.90	12.69	−101	5.60	2.17	12	0.16
4.00	8.41	−136	2.19	3.77	55	0.44
4.10	5.30	−125	0.73	7.64	98	1.52
4.20	4.09	− 98	0.39	13.55	139	4.11

III. Effect on Amplitude-Frequency Characteristics

The LNC consists of a low-noise amplifier (LNA) and a down-converter. Normally, the forward gain of the LNA is around 50 dB and the backward loss is approximately 80 dB. The difference is 30 dB. Therefore, the input reflective index of the down-converter almost has no contribution to that of the LNC. The input reflective index of the LNC is that of the LNA.

The power transmission gain of the LNA can be expressed as

$$G_T = G_1(1-|\Gamma_{in}|^2)G \tag{1}$$

where G is the actual power gain, Γ_{in} is the input reflective index, and G_1 is

$$G_1 = (1-|\Gamma_1|^2)/|1-\Gamma_1\Gamma_{in}|^2 \tag{2}$$

it depends on the source reflective index Γ_1. Ideally, $|\Gamma_1| = 0$ and $G_1 = 1$. When the LNC operates behind the feeder, the reflective index of the feeder is usually not equal to zero. Thus, the gain would fluctuate. If the mode of Γ_1 remains essentially unchanged with frequency and only its frequency varies, then the maximum gain fluctuation ΔG_{1max} is

$$\Delta G_{1max}(\text{dB}) = 20\log\{(1+|\Gamma_1\Gamma_{in}|)/(1-|\Gamma_1\Gamma_{in}|)\} \approx 17.4|\Gamma_1\Gamma_{in}| \tag{3}$$

Thus, the maximum gain fluctuation values for different $|\Gamma_1|$ and $|\Gamma_{in}|$ can be obtained using this equation, as shown in Table 2.

Table 2. Maximum Values of Additional Gain Fluctuation

$\lvert\Gamma_1\rvert$ \ $\lvert\Gamma_{in}\rvert$		0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8
$\lvert\Gamma_1\rvert$	$VSWR_1$ \ $VSWR_{in}$	1.25	1.5	1.9	2.3	3.0	4.0	5.7	9.0
0.091	1.2	0.16	0.32	0.48	0.64	0.73	0.94	1.10	1.26
0.13	1.3	0.22	0.46	0.68	0.90	1.14	1.36	1.58	1.81

[Passage omitted]

V. Conclusions

This paper only analyzed the effect of input VSWR of LNC on the stability, amplitude-frequency response and carrier-to-noise ratio C/N of the system. Based on our preliminary analysis, when the input VSWR of the LNC is less than 3 and the input VSWR of the antenna-fed system is under 1.2, the additional gain fluctuation introduced is less than 0.78 dB. The input VSWR of the LNC has no direct contribution to the carrier-to-noise ratio C/N. It should be separated from the uncertainty of noise-temperature measurement. When the input end of the LNC is not equipped with an insulator, its noise temperature is dependent upon the reflective index of the antenna-fed system. When its VSWR is 1.3, the operating noise temperature of the LNC may differ by 20°K.

The input VSWR of the LNC also affects the time delay, differential gain and differential phase of the system. These effects are not discussed in this paper. Nevertheless, they are insignificant compared to long-range microwave relay communications because they are not cumulative from station to station.

Table 6 shows results of the input VSWR of the LNC with different insulators for C-band satellite television earth stations abroad. The data in the table were measured using an improved HP8410C S-parameter testing system. The MSE Company's LA4880 LNA and HYTEK's LNA are already in use at several domestic earth stations. The Toshiba LNB-C1 was a 1986 product. TW-86001-86003 are low-noise amplifiers for C-band satellite earth stations; these LNA's were developed by Qinghua University.

Table 6. Results of Input VSWR of Several LNC's

Model / Frequency	MSE LA4880 581988	MSE LA4880 512832	TOSHIBA LNB-C1 001078	HYTEK 5291514	TW 86001	TW 86002	TW 86003
3.7	1.91	2.48	2.43	2.57	1.25	1.24	1.02
3.8	2.55	3.22	2.40	2.57	1.37	1.34	1.12
3.9	3.86	3.64	1.73	3.02	1.52	1.48	1.80
4.0	2.50	3.99	2.13	2.34	1.69	1.68	1.59
4.1	3.86	4.12	2.52	2.22	1.83	1.94	1.81
4.2	3.90	4.17	4.00	3.20	1.98	2.33	1.92

Based on both theoretical analysis and practical application, we believe it is necessary to impose strict specifications on the input VSWR of an LNC for a satellite earth station. We can divide them into different grades to meet the needs of different satellite earth stations to reduce cost.

[Passage omitted]

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High-Efficiency Time-Slot Assignment Algorithm for SS-TDMA System

40080113d Beijing TONGXIN XUEBAO [JOURNAL OF CHINA INSTITUTE OF COMMUNICATIONS] in Chinese Vol 9 No 6, Nov 88 pp 79-87

[Article by Bi Duyan* [3968 4648 1750], Liu Guoliang* [0491 0948 2856] and Zhou Zhaoqi* [0719 0340 4388]: "High-Efficiency Time-Slot Assignment Algorithm for the SS-TDMA System"; manuscript received 14 Oct 86]

[Excerpts] Abstract

This paper first briefly describes the architecture and operating principle of the SS-TDMA satellite communications system and then discusses a time-slot assignment algorithm for the system. Based on an analysis of existing time-slot algorithms, a highly-efficient time-slot assignment (HEA) algorithm is presented. Compared to the TSA-2 algorithm, the number of modes is reduced by an average of 37.8 percent. Its complexity is $O(N^{4.5} \log_2 N)$. Compared to the complexity of the TSA-2 algorithm, which is $O(N^5)$, calculation time is reduced by several hundred percent.

I. Introduction

The SS-TDMA (satellite-switched--time division multiple access) system is a recently developed high-capacity, flexible satellite communications system with a high transponder utilization rate. Its architecture is shown in Figure 1.

* Bi Duyan: Assistant Professor at the Air Force College of Engineering, Xian. He received his Master's degree in electronic technology in Jan. 1986 from the University of Science and Technology for National Defense and is engaged in digital image processing research.

Liu Guoliang: Associate Professor in the information engineering department of Xidian University, Xian.

Zhou Zhaoqi: Professor at the University of Science and Technology for National Defense, Changsha.

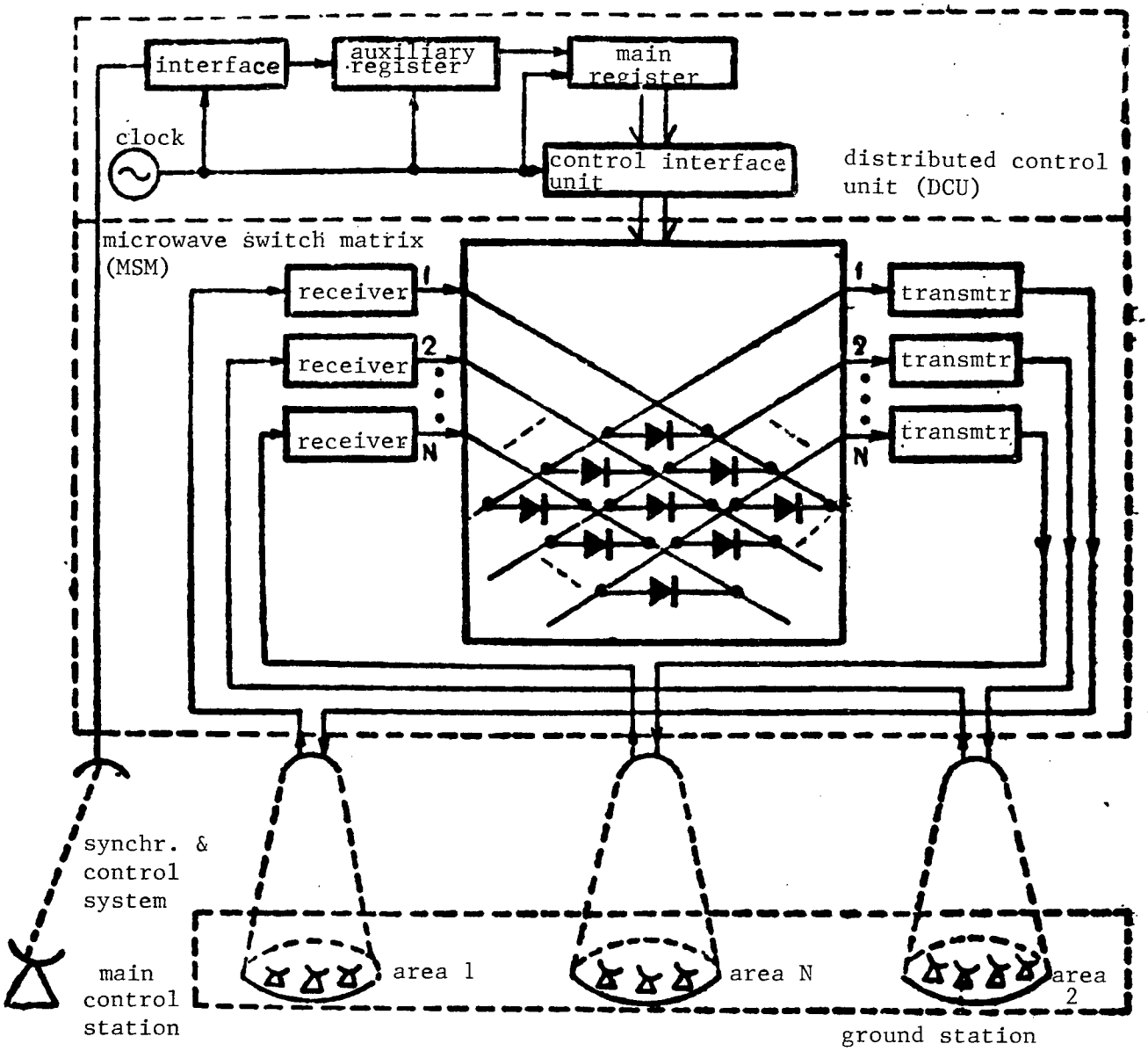

Figure 1 Block diagram of the SS-TDMA system

The satellite of the system has multiple beams covering different regions on earth. In order to establish a connection between regions covered by individual beams, the satellite is equipped with a microwave switch matrix (MSM) and distributed control unit (DCU). The ground facilities include a main control station and several TDMA stations located in various areas covered by the beams. Based on the demand of each station, the main control station assigns the connection sequence for the MSM and the burst time for each station. The assignment provided by the main control station is sent to the auxiliary register of each DCU via the telemetry, tracking and control (TT&C) circuit. It is then sent to the main register after it is verified. In addition,

the main control station also transmits the assignment to every earth station via communication lines. Finally, the assigned connection sequence is made by the microwave diode of the MSM which is controlled by the DCU. Each ground station bursts at the scheduled time to transfer information between stations based on demand.

In order to utilize the transponder efficiently, a connection sequence for the MSM and the burst time for each ground station must be assigned in a timely manner; this is called time-slot assignment. Since the burst time for each ground station can be calculated using a conventional algorithm for TDMA, the time-slot assignment we are concerned with is the assignment of the MSM connection sequence.

Several time-slot algorithms have been introduced[2-5]. The most predominant ones are the Greedy algorithm introduced by Y. Ito and the TSA-2 algorithm introduced by T. Inukai. The upper limit of the number of modes for an NxN switch matrix is N^2-N, using the Greedy algorithm. In the worst case, the complexity of operation is O(N!). The TSA-2 algorithm has a maximum number of modes of N^2-2N+2 and complexity of $O(N^5)$. Therefore, the TSA-2 algorithm is obviously superior to the Greedy algorithm. In a small SS-TDMA system, where N, the number of areas covered by the beams, is small, the TSA-2 algorithm works well. However, in a large SS-TDMA system where N is large, the number of modes generated by the TSA-2 algorithm increases and the speed of computation slows down significantly. In this paper, based on the TSA-2 algorithm, a highly efficient assignment (HEA) algorithm suitable not only for small but also for large SS-TDMA systems is proposed. On an average, the number of modes produced is reduced by 37.8 percent compared to that of the TSA-2 algorithm. The upper limit of the number of modes of HEA is identical to that of TSA-2, i.e. N^2-2N+2. The complexity of operation is $O(N^{4.5}\log_2 N)$ for HEA, which is lower than that of the TSA-2 algorithm and even lower than that of the Greedy algorithm.

For convenience, the mathematical model of the time-slot assignment is provided first. Then, conclusion (1) is given. It is followed by two improvements, i.e. DM (Decreasing Modes) and FS (Fast Speed). Finally, the HEA algorithm is introduced and simulation results using different algorithms are shown.

II. Introduction to Time-Slot Assignment

Let d_{ij} represent the traffic to be transmitted from an area covered by beam i to an area covered by beam j. The variable d_{ij} is always an integer; it represents the time-slot number or channel number in one frame. In an SS-TDMA system with N areas, each covered by a beam we can set up a matrix with all the values of d_{ij} as shown in Figure 2. It is the switch matrix which represents the total traffic of the system. The row and column numbers represent the transmitting and receiving area, respectively. The sum of d_{ij} over all row numbers,

$$\sum_{j=1}^{N} d_{ij} = S_i$$

is the total traffic to be transmitted by the area covered by beam i to itself (between stations covered by the same beam) and areas covered by other beams. The sum of d_{ij} over all column numbers,

$$\sum_{i=1}^{N} d_{ij} = R_j$$

is the total traffic to be received by the area covered by beam j from itself and areas covered by other beams.

receive

transmit

	1	2	• • •	N	$\sum_j d_{ij}$
1	d_{11}	d_{12}	• • •	d_{1N}	S_1
2	d_{21}	d_{22}	• • •	d_{2N}	S_2
•	•	•	•	•	•
N	d_{N1}	d_{N2}	• • •	d_{NN}	S_N
$\sum_i d_{ij}$	R_1	R_2	• • •	R_N	

Figure 2. Switch Matrix

The switch matrix $|d_{ij}|$ is denoted as D. The mathematical model for time-slot assignment can be expressed as follows:

Let us express the switch matrix D as the sum of a series of matrices D_i, i.e.,

$$D = D_1 + D_2 + \ldots\ldots + D_{11} \qquad (A)$$

Moreover, the decomposition process satisfies the following conditions:

(1) The state matrix D_i (i=1,2,....,k) has no more than one non-zero element per row or column.

(2) The number of matrices, i.e. the number of modes, is the minimum

(3) The sum of the maximum element for each D_i (which is denoted as $|D_i|_m$), i.e., $T' = \sum_{i=1}^{k} |D_i|_m$, is the minimum.

(4) The rate of decomposition is as fast as possible.

Every D_i corresponds to a MSM connection state. An array of D_i forms a switch sequence. Condition (1) ensures a one-to-one correspondence between each area when MSM is in state i. Condition (2) minimizes the number of MSM connection states, i.e. the number of modes. Consequently, it minimizes the MSM transition time due to switching. Condition (3) can reduce the actual frame length to improve efficiency. Condition (4) was introduced to ensure the timely transmission of information.

There are three parameters that can be used to evaluate a time-slot assignment algorithm, i.e., assignment efficiency η ($\eta = T_m / T$, $\leq 100\%$, where $T_m = \max_{i=1,2...} \{S_i, R_i\}$); mode number k; and complexity of operation $O(N^x)$, where N is the number of beam areas.

For an optimal time-slot assignment, we should make $\eta = 100\%$, $k = k_{min}$, and $x = x_{min}$. However, it is difficult to achieve all of them at the same time. Therefore, a quasi-optimization algorithm is usually used in practice. Usually, we first make sure that $\eta = 100\%$ and relax k to x to some extent. The Greedy algorithm, and TSA-2 algorithm described earlier are both quasi-optimization algorithms. Similarly, the HEA algorithm presented here is also a quasi-optimization algorithm, however, the HEA algorithm outperforms the other two algorithms. [Passage omitted]

c. High-Efficiency Assignment Algorithm HEA

In the DM algorithm, the mode number is reduced by ensuring that each $V_{Ai'}$ is a maximum. Is it a general condition? An analysis of equations (A) and (2) shows that it is even more general to ensure that every D_i' is a maximum. In this case, the number of modes can be further reduced. Based on equation (A), if every D_i' is as large as possible, the number of D_i' is minimized. Based on (2) of equation (2), if every D_i' is a maximum, it takes the least number of times for $D^{(i'+1)}$ to approach zero. Hence, the number of modes produced can be minimized. Another important aspect is that a maximum D_i' includes the requirement that $V_{Ai'}$ is a maximum (from (1) of equation (2)). Furthermore, a maximum D_i' also requires that each SDR corresponding element d_{ij} is a maximum. Therefore, it is a more general condition to require that D_i' be maximized every time. When this condition is guaranteed, the number of modes produced is minimized. The high-efficiency HEA algorithm, which guarantees that each D_i' is a maximum by quasi-optimization, is introduced as follows.

The HEA Algorithm:

step 0: set $i' = 1$, $T_{m1} = T_m$, $D^{(1)} = D$

step 1: from the switch matrix $D^{(i')} = (d_{ij})$ and structure matrix $D^{(i')} = (d'ij)$, let

$$d_{ij} = \begin{cases} d_{ij} & \text{when } d_{ij} \text{ is on the primary line of } D^{(i')} \\ 1 & \text{when } d_{ij} \text{ is not on the primary line of } D^{(i')}. \end{cases}$$

Use the $O(N^{2.5}\log_2 N)$ max-min SDR algorithm to find a max-min SDR and note the selected elements $d_{ij} \in$ max-min SDR on the primary line.

step 2: starting from the largest non-primary line of $D^{(i')}$, find the position of the largest element as the position of its representative element. If a representative element already exists, find the representative element for the next non-primary line. If the maximum element is 0, it should be selected until the process is completed.

step 3: same as step 3 of the FS algorithm.

step 4: same as step 4 of the FS algorithm.

The primary and non-primary lines are separated in this algorithm. Each d_{ij} on the primary line is made as large as possible. In addition, the first part of $V_{Ai'}$ is also maximized. Each d_{ij} on the non-primary line is made as large as possible. Since the d_{ij} on a non-primary line of greater value is given the priority to be as large as possible, the second part of $V_{Ai'}$ is maximized. Thus, the HEA algorithm can maximize every $D_{i'}$ through a quasi-optimization process. Hence, the number of modes produced is significantly reduced as compared to that produced by the TSA-2 algorithm. Results showed that on average, the HEA algorithm produces 37.8 percent less modes than TSA-2. In terms of speed, the complexity of HEA is $O(N^{4.5}\log_2 N)$[1], compared to $O(N^5)$ for TSA-2. Based on $\lim_{N \to \infty}(N^{4.5}\log_2 N/N^5) = \lim_{N \to \infty}(\log_2 N/N^{0.5}) = 0$, the speed of HEA is several times faster than that of TSA-2 when N is relatively large.

The execution of the HEA algorithm is illustrated in the following example.

Example 2

Assume the switch matrix is

$$D = \begin{array}{|c|c|c|} \hline 10 & 3 & 8 \\ \hline 0 & 1 & 2 \\ \hline 4 & 7 & 3 \\ \hline \end{array}$$

[solution] The value of each line is calculated:

$$D = \begin{array}{|c|c|c|c|} \hline 10 & 3 & 8 & 21 \\ \hline 0 & 1 & 2 & 3 \\ \hline 4 & 7 & 3 & 14 \\ \hline 14 & 11 & 13 & \\ \hline \end{array}$$

Obviously, line 1 is the primary line and $T_m = 21$.

step 1: Construct $D^{(1)'}$:

$$D^{(1)'} = \begin{array}{|c|c|c|} \hline 10 & 3 & 8 \\ \hline 1 & 1 & 1 \\ \hline 1 & 1 & 1 \\ \hline \end{array}$$

and the max-min SDR is (1,1), (2,2) and (3,3). The SDR element on the primary line is (1,1) and its value is 10.

step 2: Find representative elements on non-primary lines. The representative element for row 3, the non-primary line with the largest value, is (3,2) and its value is 7. The first column already has a representative element and need not be considered. The next non-primary line is column 3 and its representative element position is (2,3) and the element is 2.

step 3: Calculate V_{A1}.

$$V_{A1} = \min\{d_{11}, \min\{21-(S_3-d_{32}), 21-(R_2-d_{32}), 21-(S_2-d_{23}), 21-(R_3-d_{23})\}\}$$
$$= \min\{10, \min\{21-7, 21-4, 21-1, 21-11\}\} = 10$$

$$D_1 = \min\{V_{A1}, [I^n], [d_{ij}]\} = \begin{array}{|c|c|c|} \hline 10 & & \\ \hline & & 2 \\ \hline & 7 & \\ \hline \end{array} \qquad D^{(2)} = D - D_1 = \begin{array}{|c|c|c|} \hline 0 & 3 & 8 \\ \hline 0 & 1 & 0 \\ \hline 4 & 0 & 3 \\ \hline \end{array}$$

21

step 4: Obviously, $D^2 \neq 0$. Let $D = D^2$ and go back to step 1. After three cycles, the assignment becomes.

$$D = \begin{bmatrix} 10 & & \\ & & 2 \\ & 7 & \end{bmatrix} + \begin{bmatrix} & & 8 \\ & 1 & \\ 4 & & \end{bmatrix} + \begin{bmatrix} & 3 & \\ 0 & & \\ & & 3 \end{bmatrix} = D_1 + D_2 + D_3$$

If we use the DM algorithm to solve this problem, it will result in four modes. With the TSA-2 algorithm, it will produce at least four modes.

IV. Simulation of Algorithms

All the methods discussed above, including DM, HEA and TSA-2, were simulated on an IBM-PC. The results are essentially the same as those derived theoretically. Table 1 shows the results. N is the number of beam-covered areas, i.e. the order of the switch matrix. x_0, R and C are the initial conditions for the determination of the uniform random switch matrix by multiplicative congruence. The equations are $x_n \equiv x_{n-1} R + C$ (M is mode) and $d_{ij} = \text{INT}\,[(x_n/M) \times 1000]$. In the program it program it is chosen that M = 1024. Thus, d_{ij} is a random integer uniformly distributed between 0 and 1000. The running time for the FS algorithm can be obtained from HEA since the complexity is identical.

We noticed that when N is small the number of modes generated by HEA and DM is reduced by some degree. However, the reduction is not significant. When N is large, the number of modes produced by HEA and DM is greatly decreased compared to that produced by TSA-2. This is in agreement with the theoretical conclusion described earlier.

It should also be noted that there are a few exceptions in the simulation results. When N is small, because the number of operations is low, the choice of SDR is limited. Therefore, the advantages of HEA and DM are not obvious. Consequently, we noticed that the three algorithms produced the same number of modes for N = 5 and 6. When N is larger, exceptions only occurred at N = 31 and 25. When N = 31, since except for the element in the (1,1) position, which is 549, all the remaining elements of the switch matrix D are 612, it is easy to figure out that the low limit of modes for this matrix is 31. Our results showed that this lower limit was achieved by DM, HEA and TSA-2. Hence, it is normal at N = 31. In terms of time, because TSA-2 uses the SDR

Table 1. Simulation Results

N	X_c	R	C	TSA-2	DM	HEA
Modes produced in every algorithm						
4	0	17	3	7	6	6
5	1	25	5	8	8	8
6	3	21	1	15	15	15
7	0	125	11	13	9	9
8	2	125	7	18	16	14
9	3	125	9	27	21	24
10	14	9	27	32	24	25
11	10	5	11	35	25	20
12	12	9	5	29	18	17
13	2	33	19	57	30	31
14	3	37	29	75	39	47
15	100	41	23	59	33	35
16	201	5	73	65	32	32
17	1000	25	3	38	35	36
18	333	21	31	72	38	32
19	12	25	33	96	44	44
20	1	41	11	105	51	45
21	32	101	5	98	45	39
22	12	37	19	81	40	41
23	123	45	67	106	52	43
24	234	61	79	83	43	36
25	112	108	45	25	27	27
26	245	9	3	142	59	50
27	105	81	7	140	68	60
28	508	13	11	194	72	69
29	99	49	29	155	70	62
30	468	25	1	163	58	50
31	200	192	51	31	31	31
32	16	113	7	260	97	86
33	53	21	11	196	61	55
34	1	5	9	256	79	75
35	14	25	77	226	82	65
Excution time of every algorithm						
31	200	192	51	1	11	2
32	16	113	7	10	31	3
33	53	21	11	10	22	2
34	1	5	9	11	31	3
35	14	25	77	12	35	3

algorithm and HEA uses the max-min SDR algorithm, it takes HEA a few more operations than TSA-2 to deal with a special matrix D when the SDR is extremely easy to find. Therefore, HEA was slightly slower than TSA-2. However, this is a special case when TSA-2 and HEA did not reach their upper limits of operations of N^5 and $N^{4,5} \log_2 N$, respectively. When N = 25, the switch matrix is as shown in Figure 4. Many elements are identical. However, because its primary line value is quite different from the non-primary line value, there is a great deal of flexibility in selecting the SDR elements. In HEA, the selection follows certain rules and begins with the non-primary line of largest value. the TSA-2 algorithm is more flexible. It may be possible to find the optimal selection to lower the number of modes. However, because of its superiority, the number of modes generated by HEA would not be much higher than that of TSA-2. In this example, TSA-2 is only 2 modes fewer than HEA. In this study, we have estimated that the probability for this type of special matrix to occur is very low. In reality, it is not probable that each beam-covered area has the same traffic. Otherwise, it does not require any assignment. Therefore, the two special cases do not have any impact on the superiority of HEA.

856	540	368	805	55		55
55	55	55	55	55		55
55	55	55	55	55		55
55	55	55	55	55		55

Figure 4. Switch Matrix D at N = 25

V. Conclusions

Based on the time-slot assignment model for the SS-TDMA system and the TSA-2 algorithm, we first proposed two initial improved algorithms. Then, by using the advantages of those algorithms, a high-efficiency time-slot assignment algorithm was obtained. The advantages of this algorithm are illustrated in the simulation results.

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